Asus Aaeon COM-SKUC6 User Manual

Com express module

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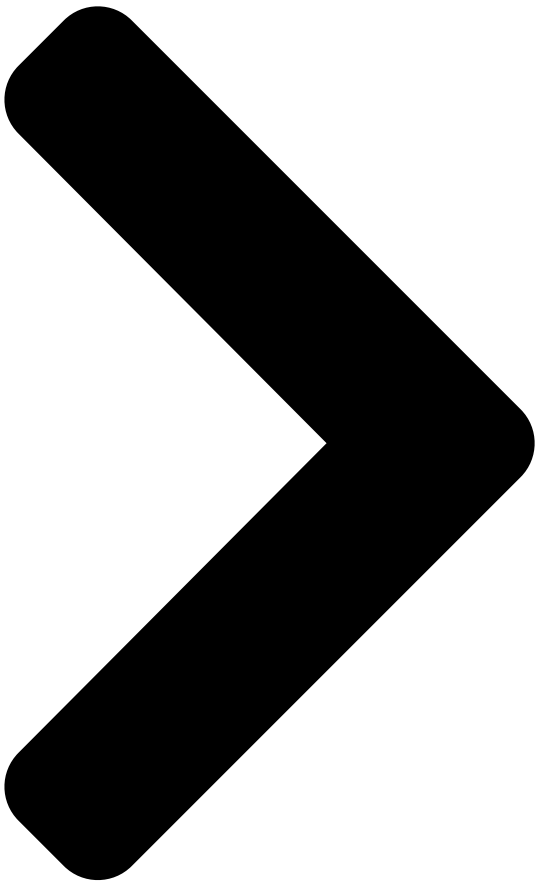

COM-SKUC6 & COM-KBUC6

COM Express Module

User's Manual 2nd Ed

Last Updated: March 4, 2019

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Related Manuals for Asus Aaeon COM-SKUC6

Control Unit Asus AAEON COM-SKUC6 User Manual

Com express module (100 pages)

Control Unit Asus AAEON COM-WHUC6 User Manual

Com express module (110 pages)

Control Unit Asus AAEON COM-BYTC2 User Manual

Com express module (91 pages)

Control Unit Asus AAEON COM-BT-A30 User Manual

Com express module (98 pages)

Control Unit Asus AAEON COM-TGHB6 User Manual

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Control Unit Asus AAEON COM-SKHB6 User Manual

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Control Unit Asus AAEON COM-TGUC6 User Manual

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Control Unit Asus Aaeon NanoCOM-APL User Manual

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Control Unit Asus ThunderboltEX 3-TR User Manual

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Control Unit Asus TPM-SPI Quick Start Manual

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Control Unit Asus AAEON MIPICSI Camera RVP Converter Kit User Manual

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Control Unit Asus Aaeon NanoCOM-TGU User Manual

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Control Unit Asus Aaeon NIM-S26B Quick Installation Manual

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Summary of Contents for Asus Aaeon COM-SKUC6

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Page 3 Acknowledgement All other products' name or trademarks are properties of their respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. Intel, Pentium, Celeron, and Xeon are registered trademarks of Intel Corporation Core, Atom are trademarks of Intel Corporation ...

Page 4 Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity COM-SKUC6 or COM-KBUC6 M2.5 screws If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

Page 5 About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the AAEON.com for the latest version of this document.

Page 6 Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

Page 7 If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

Page 8 FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Page 9 China RoHS Requirements (CN) □□□□□□□□□□□□□□□□□□ AAEON Main Board/ Daughter Board/ Backplane □□□□□□□□□ □□□□ □ □ □ □□□ □□□□ □□□□□ (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) □□□ □□ ○ ○ ○ ○ ○ ○ □□□□□□ □□□□ ○ ○ ○ ○ ○ ○ □□□□□□...

Page 10 China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Main Board/ Daughter Board/ Backplane Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) PCB &...

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Page 14: Chapter 1 - Product Specifications

Chapter 1 Chapter 1 - Product Specifications...

Page 15: Specifications

Specifications System COM Express Compact Size, Type 6 Form Factor Onboard 6th/7th Generation Intel® Core™ U-series Processor, BGA type Up to i7-7600U 2C/ 2.8 GHz CPU Frequency Onboard 6th/7th Generation Intel® Core™ Chipset U-series Processor DDR3L 1600, SODIMM x 1 Memory Type 8 GB Max.

Page 16 System 182,306 hrs. MTBF (Hours) CE/FCC Class A Certification Display VGA/LCD Controller Onboard 6th Gen Intel® Core™ U-series Processor, GT2-520/510 Onboard 7th Gen Intel® Core™ U-series Processor, GT2-620/610 Video Output VGA, LVDS/eDP, DDI x 1 (up to 2) Intel® PHY I219LM, Giga LAN (Support Intel® Ethernet AMT 12.0) x 1 HD Audio...

Page 17: Chapter 2 - Hardware Information

Chapter 2 Chapter 2 – Hardware Information...

Page 18: Dimensions, Jumpers And Connectors

Dimensions, Jumpers and Connectors Component Side Chapter 2 – Hardware Information Component Side...

Page 19 Solder Side Solder Side Chapter 2 – Hardware Information...

Page 20 With Heat spreader Chapter 2 – Hardware Information...

Page 21: List Of Jumpers

List of Jumpers Please refer to the table below for all of the board's jumpers that you can configure for your application Label Function AT/ATX switch & DDI/VGA switch DIMM1 DDR3L Socket ROW A/B ROW C/D RTC Connector SPI ROM FLASH 2.2.1 AT/ATX Switch &...

Page 22 Row A Row B Signal Signal GBE0_MDI2+ LPC_AD3 GBE0_LINK GBE0_MDI1- GBE0_MDI1+ LPC_CLK GND (FIXED) GND (FIXED) GBE0_MDI0- PWRBTN# GBE0_MDI0+ SMB_CK GBE0_CTREF SMB_DAT SUS_S3# SMB_ALERT# SATA0_TX+ SATA1_TX+ SATA0_TX- SATA1_TX- SUS_S4# SUS_STAT# SATA0_RX+ SATA1_RX+ SATA0_RX- SATA1_RX- GND (FIXED) GND (FIXED) SATA2_TX+ (note) SATA2_TX- (note) SUS_S5# PWR_OK...

Page 23 Row A Row B Signal Signal BIOS_DIS0# I2C_DAT THRMTRIP# USB6- USB7- USB6+ USB7+ USB_6_7_OC# USB_4_5_OC# USB4- USB5- USB4+ USB5+ GND (FIXED) GND (FIXED) USB2- USB3- USB2+ USB3+ USB_2_3_OC# USB_0_1_OC# USB0- USB1- USB0+ USB1+ VCC_RTC EXCD1_PERST# EXCD0_PERST# EXCD1_CPPE# EXCD0_CPPE# SYS_RESET# LPC_SERIRQ CB_RESET# GND (FIXED) GND (FIXED)

Page 24 Row A Row B Signal Signal PCIE_TX2+ PCIE_RX2+ PCIE_TX2- PCIE_RX2- GPI1 GPO3 PCIE_TX1+ PCIE_RX1+ PCIE_TX1- PCIE_RX1- WAKE0# GPI2 WAKE1# PCIE_TX0+ PCIE_RX0+ PCIE_TX0- PCIE_RX0- GND (FIXED) GND (FIXED) LVDS_A0+ LVDS_B0+ LVDS_A0- LVDS_B0- LVDS_A1+ LVDS_B1+ LVDS_A1- LVDS_B1- LVDS_A2+ LVDS_B2+ LVDS_A2- LVDS_B2- LVDS_VDD_EN LVDS_B3+ LVDS_A3+ LVDS_B3-...

Page 25 Row A Row B Signal Signal PCIE0_CK_REF+ BISO_DIS1# PCIE0_CK_REF- VGA_RED GND (FIXED) GND (FIXED) +V3.3S(option) VGA_GRN SPI_MISO VGA_BLU GPO0 VGA_HSYNC SPI_CLK VGA_VSYNC SPI_MOSI VGA_I2C_CK VGA_I2C_DAT SPI_CS# CB_STXD1X SMI# CB_SRXD1X SCI# A100 GND (FIXED) B100 GND (FIXED) A101 CB_STXD2X B101 CB_FAN_PWM A102 CB_SRXD2X B102...

Page 26: Row C/D Connector (Cn2)

2.2.3 ROW C/D Connector (CN2) Row C Row D Signal Signal GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) USB_SSRX0- USB_SSTX0- USB_SSRX0+ USB_SSTX0+ GND (FIXED) GND (FIXED) USB_SSRX1- USB_SSTX1- USB_SSRX1+ USB_SSTX1+ GND (FIXED) GND (FIXED) USB_SSRX2- USB_SSTX2- USB_SSRX2+ USB_SSTX2+ GND (FIXED) GND (FIXED) USB_SSRX3- USB_SSTX3-...

Page 27 RSVD DDI1_PAIR0+ RSVD DDI1_PAIR0- RSVD RSVD DDI1_PAIR1+ DDI1_PAIR1- GND (FIXED) GND (FIXED) DDI2_CTRLCLK_AUX+ DDI1_PAIR2+ DDI2_CTRLDATA_AUX- DDI1_PAIR2- DDI2_DDC_AUX_SEL DDI1_DDC_AUX_SEL RSVD RSVD DDI1_PAIR3+ DDI1_PAIR3- RSVD DDI2_PAIR0+ DDI2_PAIR0- GND (FIXED) GND (FIXED) DDI2_PAIR1+ DDI2_PAIR1- DDI1_HPD RSVD RSVD DDI2_PAIR2+ DDI2_PAIR2- RSVD RSVD DDI2_PAIR3+ DDI2_PAIR3- GND (FIXED) GND (FIXED) Chapter 2 –...

Page 28 GND (FIXED) GND (FIXED) RSVD RSVD RSVD RSVD RSVD GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) RSVD RSVD GND (FIXED) GND

(FIXED) Chapter 2 – Hardware Information...

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RSVD RSVD GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) RSVD RSVD C100 GND (FIXED) D100 GND (FIXED) C101 D101 C102 D102 C103 GND (FIXED) D103 C104 VCC_12V D104 VCC_12V C105 VCC_12V D105 VCC_12V C106...

Page 30: Rtc Connector (Cn3)

2.2.4 RTC Connector (CN3) Signal Battery power 2.2.5 SPI ROM FLASH (CN4) Signal SPI_SO_F SPI_CLK_F 3.3V SPI_SI_F SPI_CE0#_F SPI_CE1#_F Chapter 2 – Hardware Information...

Page 31: Chapter 3 - Ami Bios Setup

Chapter 3 Chapter 3 - AMI BIOS Setup...

Page 32: System Test And Initialization

System Test and Initialization The board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

Page 33: Ami Bios Setup

AMI BIOS Setup The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off. To enter Setup, power on the computer and press <Del>or <ESC>...

Page 34: Setup Submenu: Main

Setup submenu: Main Chapter 3 – AMI BIOS Setup...

Page 35: Setup Submenu: Advanced

Setup submenu: Advanced Chapter 3 – AMI BIOS Setup...

Page 36: Advanced: Cpu Configuration

3.4.1 Advanced: CPU Configuration Options Summary Hyper-Threading Disabled Enabled Optimal Default, Failsafe Default Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). Intel (VMX) Disabled Virtualization Enabled Optimal Default, Failsafe Default Technology When enabled, a VMM can utilize the additional hardware capabilities provided by...

Page 37: Advanced: Sata Configuration

3.4.2 Advanced: SATA Configuration Options Summary SATA Controller(s) Enabled Optimal Default, Failsafe Default Disabled Enable/Disable SATA Device. SATA Controller Auto Optimal Default, Failsafe Default Speed Gen1 Gen2 Gen3 Indicates the maximum speed the SATA controller can support. Port 0 Disabled Enabled Optimal Default, Failsafe Default Enable or Disable SATA Port.

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Options Summary Port 1 Disabled Enabled Optimal Default, Failsafe Default Enable or Disable SATA Port. Hot Plug Disabled Optimal Default, Failsafe Default Enabled Designates this port as Hot Pluggable. Port 2 Disabled Enabled Optimal Default, Failsafe Default Enable or Disable SATA Port. Hot Plug Disabled Optimal Default, Failsafe Default...

Page 39: Advanced: Usb Configuration

3.4.3 Advanced: USB Configuration Options summary: Options Summary Legacy USB Support Enabled Optimal Default, Failsafe Default Disabled Auto Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI application. Chapter 3 –...

Page 40: Advanced: On-Module Features

3.4.4 Advanced: On-Module FEATURES Options Summary Battery Disabled Optimal Default, Failsafe Default Management One Battery Enabled to support battery in ACPI OS by I2C_CK ,

I2C_DAT (B33,B34) Chapter 3 – AMI BIOS Setup...

Page 41: Advanced: Sio Configuration

3.4.5 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

Page 42: Sio Configuration: Serial Port 9 Configuration

3.4.5.1 SIO Configuration: Serial Port 9 Configuration Options Summary Use This Device Disabled Enabled Optimal Default, Failsafe Default Enabled or Disabled this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2D8h; IRQ=11; DMA; IO=2C8h; IRQ=11; DMA; Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

Page 43: Sio Configuration: Serial Port 10 Configuration

3.4.5.2 SIO Configuration: Serial Port 10 Configuration Options Summary Use This Device Disabled Enabled Optimal Default, Failsafe Default Enabled or Disabled this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2C8h; IRQ=10; DMA; IO=2D8h; IRQ=10; DMA; Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

Page 44: Advanced: Power Management

3.4.6 Advanced: Power Management Options Summary Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select system power mode. Restore AC Power Last State Loss Always On Always Off Optimal Default, Failsafe Default Wake on LAN Enabled Optimal Default, Failsafe Default Enable Disabled Enabled/ Disabled integrated LAN to wake the system.

Page 45: Advanced: Digital Io Port Configuration

3.4.7 Advanced: Digital IO Port Configuration Options Summary GPI * Input Optimal Default, Failsafe Default Output Set DIO as Input or Output Interrupt Disabled Optimal Default, Failsafe Default Enabled Enabled interrupt function with low pulse mode. This triggered pulse needs more then the 10ms.

Page 46: Advanced: On-Module Hardware Monitor

3.4.8 Advanced: On-Module Hardware Monitor Chapter 3 – AMI BIOS Setup...

Page 47: Fan 1 Mode Configuration: Cpu Smart Fan Full Mode

3.4.8.1 Fan 1 Mode Configuration: CPU Smart Fan Full Mode Options Summary CPU Smart Fan Full Mode Optimal Default, Failsafe Default control Manual Mode by PWM Auto Mode by PWM PWM signal Non-inverting Optimal Default, Failsafe Default Inverting Select output PWM of inverting or non-uninverting signal Chapter 3 –...

Page 48: Fan 1 Mode Configuration: Cpu Smart Fan Manual Mode

3.4.8.2 Fan 1 Mode Configuration: CPU Smart Fan Manual Mode Options Summary Manual Setting Optimal Default, Failsafe Default Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number: Chapter 3 – AMI BIOS Setup...

Page 49: Fan 1 Mode Configuration: Cpu Smart Fan Auto Mode

3.4.8.3 Fan 1 Mode Configuration: CPU Smart Fan Auto Mode Options Summary Monitor Thermal CPU Temperature(DTS) Optimal Default, Failsafe Default Thermal Source 1(T1) Thermal Source 2(T2) Select monitor thermal source Temperature of Start Optimal Default, Failsafe Default Temperature Of Start Temperature Of Off Optimal Default, Failsafe Default Temperature Of Off...

Page 50: Advanced: Trusted Computing

3.4.9 Advanced: Trusted Computing Options Summary Security Device Disable Support Enable Optimal Default, Failsafe Default Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. SHA-1 PCR Bank Disable Enable Optimal Default, Failsafe Default...

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Options Summary Platform Hierarchy Disable Enable Optimal Default, Failsafe Default Enable or Disable Platform Hierarchy Storage Hierarchy Disable Enable Optimal Default,

Failsafe Default Enable or Disable Storage Hierarchy Endorsement Disable Hierarchy Enable Optimal Default, Failsafe Default Enable or Disable Endorsement Hierarchy TPM2.0 UEFI Spec TCG_2 Optimal Default, Failsafe Default...

Page 52: Advanced: Firmware Update Configuration

3.4.10 Advanced: Firmware Update Configuration Options Summary Me FW Image Disable Optimal Default, Failsafe Default Re-Flash Enable Enable/ Disable Me FW Image Re-Flash functinn. Chapter 3 – AMI BIOS Setup...

Page 53: Setup Submenu: Chipset

Setup submenu: Chipset Chapter 3 – AMI BIOS Setup...

Page 54: Chipset: System Agent (Sa) Configuration

3.5.1 Chipset: System Agent (SA) Configuration Chapter 3 – AMI BIOS Setup...

Page 55: System Agent (Sa): Graphics Configuration

3.5.1.1 System Agent (SA): Graphics Configuration Options Summary Primary Display Auto Optimal Default, Failsafe Default IGFX Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx. Primary IGFX Boot VBIOS Default Optimal Default, Failsafe Default Display DDI1/DP DDI2/VGA...

Page 56: Graphics Configuration: Lvds Panel Configuration

3.5.1.2 Graphics Configuration: LVDS Panel Configuration Options Summary Panel Type 640x480@60Hz 800x480@60Hz 800x600@60Hz 1024x600@60Hz 1024x768@60Hz Optimal Default, Failsafe Default 1280x768@60Hz 1280x800@60Hz 1280x1024@60Hz 1366x768@60Hz 1440x900@60Hz 1600x1200@60Hz 1920x1080@60Hz 1920x1200@60Hz Select panel type Chapter 3 – AMI BIOS Setup...

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Options Summary Color Depth 18-bit Optimal Default, Failsafe Default 24-bit Select Color Depth Backlight Type Normal Optimal Default, Failsafe Default Inverted Select backlight control signal type Backlight Level Optimal Default, Failsafe Default 100% Select backlight control level Backlight PWM Freq 100Hz 200Hz 220Hz...

Page 58: Chipset: Pch-Io Configuration

3.5.2 Chipset: PCH-IO Configuration Options Summary HD Audio Disabled Enabled Auto Optimal Default, Failsafe Default Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled Auto = HDA will be enabled if present, disabled otherwise. PCH LAN Enabled Optimal Default, Failsafe Default...

Page 59: Chipset: Pcie Type Switch Selection

3.5.3 Chipset: PCIE Type Switch Selection Options Summary PCIe Controller1 PCIe Port0~3 are four X1 Configuration PCIe Port0~3 is one X4 Optimal Default, Failsafe Default Select PCI Express Root Port * Selection. PCI Express Root Disabled Port 1 Enabled Optimal Default, Failsafe Default Control the PCI Express Root Port.

Page 60: Setup Submenu: Security

Setup submenu: Security Change Administrator/User Password You can set an Administrator password. If you set an Administrator password, you can then set a User password. User passwords do not have access to many of the features in the Setup utility. Select the password you want to set and press <Enter>.

Page 61: Security: Secure Boot

3.6.1 Security: Secure Boot Options Summary Attempt Secure Boot Disabled Optimal Default, Failsafe Default Enabled Secure Boot activated when Platform Key(PK) is enrolled, System mode is User/Deployed, and CSM function is disable Secure Boot Mode Standard Custom Optimal Default, Failsafe Default Secure Boot Mode selector: Standard/Custom.

Page 62: Secure Boot: Key Management

3.6.1.1 Secure Boot: Key Management Options Summary Provision Factory Disabled Optimal Default, Failsafe Default Defaults Enabled Allow to provision factory default Secure Boot keys

when System is in setup Mode Install Factory Default keys Force System to User Mode - install all Factory Default keys Enroll Efi Image Allow the image to run in Secure Boot mode.

Page 63 Options Summary Platform Key(PK) Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test Key Exchange Keys Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)

Page 64 Options Summary Forbidden Signatures Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test Authorized TimeStamps Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)

Page 65: Setup Submenu: Boot

Setup submenu: Boot Options Summary Quiet Boot Disabled Enabled Optimal Default, Failsafe Default Enables or Disables Quiet Boot option. Launch PXE Boot Disabled Optimal Default, Failsafe Default UEFI Legacy Controls the execution of UEFI and Legacy PXE OpROM. BIOS MODE UEFI and Legacy Optimal Default, Failsafe Default UEFI only...

Page 66: Boot: Hard Drive Bbs Priorities

3.7.1 Boot: Hard Drive BBS Priorities Chapter 3 – AMI BIOS Setup...

Page 67: Setup Submenu: Save & Exit

Setup submenu: Save & Exit Chapter 3 – AMI BIOS Setup...

Page 68: Chapter 4 - Drivers Installation

Chapter 4 Chapter 4 – Drivers Installation...

Page 69: Driver Download/Installation

Driver Download/Installation Drivers for the COM-KBUC6/SKUC6 can be downloaded from the product page on the AAEON website by following this link: https://www.aaeon.com/en/p/com-express-modules-com-kbuc6 Download the driver(s) you need and follow the steps below to install them. 4.1.1 COM-KBUC6 Driver Installation Steps Step 1 –...

Page 70 Step 4 – Install Audio Driver Click the STEP4 - Audio folder followed by 0008-64bit_Win7_Win8_Win81_Win10_R281.exe Follow the instructions Drivers will be installed automatically Step 5 – Install ME Driver 1. Click the STEP5 - ME folder followed by SetupME.exe 2. Follow the instructions 3.

Page 71: Com-Skuc6 Driver Installation Steps

4.1.2 COM-SKUC6 Driver Installation Steps Step 1 – Install Chipset Driver Click the Step1 - Chipset folder followed by SetupChipset.exe Follow the instructions Drivers will be installed automatically Step 2 – Install Graphics Driver Click the Step2 - Graphic folder and select your OS Click the Setup.exe file in the folder Follow the instructions Drivers will be installed automatically...

Page 72 Step 5 – Install USB 3.0 (Windows 7 only) 1. Click the STEP5 – USB 3.0 folder followed by Win7 folder 2. Click Setup.exe 3. Follow the instructions 4. Drivers will be installed automatically Step 6 – Install ME Driver Click the STEP5 - ME folder followed by Windows folder.

Page 73: Appendix A - Watchdog Timer Programming

Appendix A Appendix A - Watchdog Timer Programming...

Page 74: Watchdog Timer Initial Program

Watchdog Timer Initial Program Table 1 : Embedded BRAM relative register table Default Value Note Index 0x284(Note1) BRAM Index Register Data 0x285(Note2) BRAM Data Register Logical Device Number 0xA8(Note3) Watch dog Logical Device Number Function and Device Number

0x00(Note4) Watch dog Function/Device Number Table 2 : Watchdog relative register table Option BitNum...

Page 75 ********** // Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex //This parameter is represented from Note1 #define byte EcBRAMData //This parameter is represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3 #define byte BRAMFnDataReg //This parameter is represented from Note4 #define void EcBRAMWriteByte(byte Offset, byte Value);...

Page 76 ********** Main VOID // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) // (boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure : AaeonWDTEnable // This procudure will enable the WDT counting. AaeonWDTEnable(); ********** Appendix A – Watchdog Timer Programming...

Page 77 ********** // Procedure : AaeonWDTEnable AaeonWDTEnable () VOID WDTEnableDisable(// Procedure : AaeonWDTConfig AaeonWDTConfig () VOID // Disable WDT counting WDTEnableDisable(// WDT relative parameter setting WDTParameterSetting(); WDTEnableDisable(byte Value) VOID ECBRAMWriteByte(TimerReg , Value); WDTParameterSetting() VOID Byte TempByte; // Watchdog Timer counter setting ECBRAMWriteByte(TimerReg , TimerVal);...

Page 78 ********** ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value) VOID IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg); IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData, 0x30); //Write start ECBRAMReadByte(byte OPReg) Byte IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData, 0x10);...

Page 79: Appendix B - I/O Information

Appendix B Appendix B - I/O Information...

Page 80: I/O Address Map

I/O Address Map Appendix B – I/O Information...

Page 81: Memory Address Map

Memory Address Map Appendix B – I/O Information...

Page 82: Irq Mapping Chart

IRQ Mapping Chart Appendix B – I/O Information...

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Page 92: Appendix C - Programming Digital I/O

Appendix C Appendix C – Programming Digital I/O...

Page 93: Digital I/O Programming

Digital I/O Programming The COM-KBUC6 utilizes an AAEON chipset as its Digital I/O controller. Below are the procedures to complete its configuration, which you can use to develop a customized program to fit your application. C.2 Digital I/O Register Table 1 : Embedded BRAM relative register table Default Value Note Index...

Page 94: Digital I/O Sample Program

C.2 Digital I/O Sample Program
********** // Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex //This parameter is represented from Note1 #define byte EcBRAMData //This parameter is represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3 #define byte BRAMFnData0Reg //This parameter is represented from Note4...

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Main VOID Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin level is High PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit); // Procedure : AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...

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AaeonReadPinStatus(byte OptionReg, byte BitNum) Boolean Byte TempByte; TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg); If (TempByte & BitNum == 0) Return 0; Return 1; AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value) VOID Byte TempByte; TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg); TempByte |= (Value << BitNum); ECBRAMWriteByte(OptionReg, BitNum, Value);...

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ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value) VOID IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg); IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData, 0x30); //Write start ECBRAMReadByte(byte FnDataReg, byte OPReg) Byte IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, FnDataReg); IOWriteByte(EcBRAMIndex, 0x12);...

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Appendix D Appendix D –Notes for Users...

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Notes for Users Please observe the following items to ensure optimal performance: Always use a new SSD with the latest firmware and SATA Gen3 cable for optimal performance and compatibility. ® With the EHCI controller no longer available on the 6 Gen Intel Core™...

This manual is also suitable for:

Aaeon com-kbuc6