Operation; Cpu; Memory Map - Toshiba TLCS-90 Series Data Book

8 bit microcontroller

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

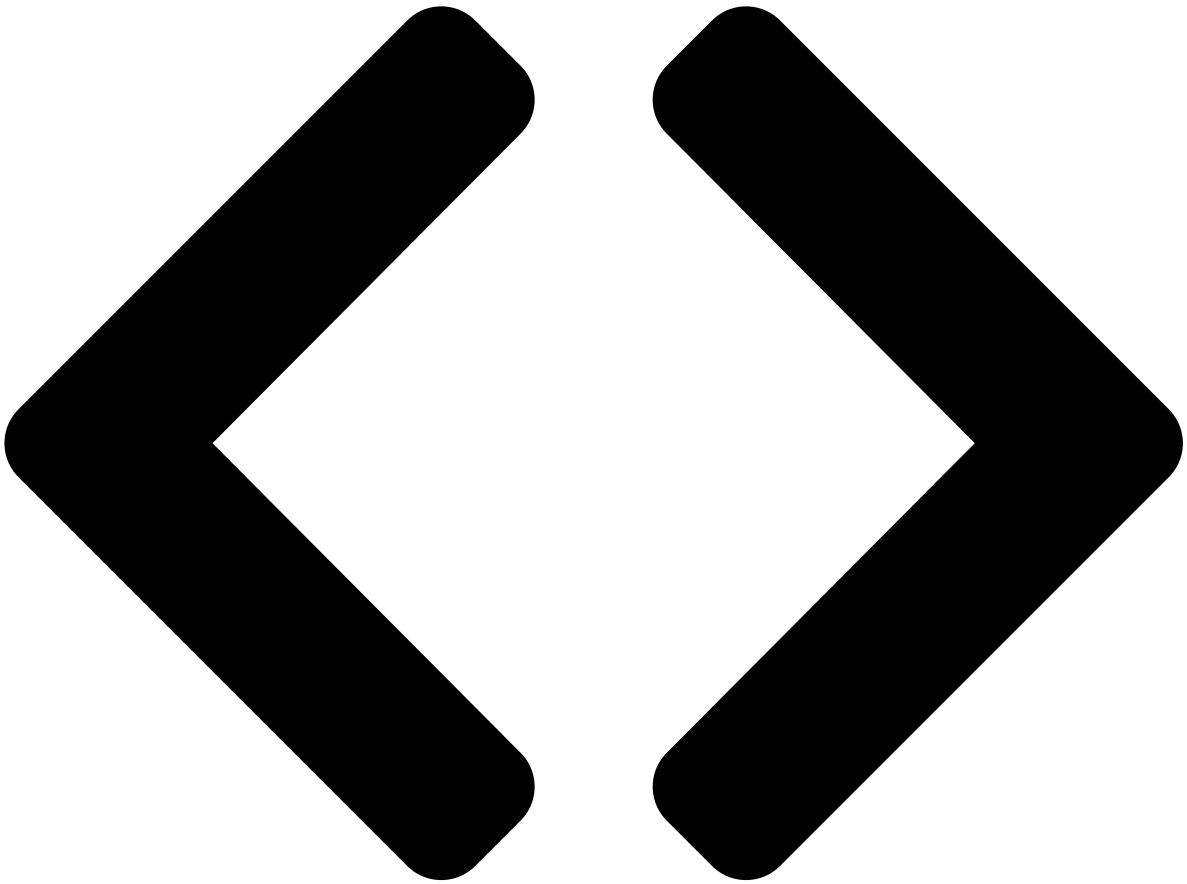
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
Table Of Contents
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217

318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364

Table of Contents

-

Bookmarks



3. OPERATION

This chapter describes the functions and the basic operations of the TMP90C840 in every block.

3.1 CPU

The TMP90C840 incorporates a high-performance 8-bit CPU.

This CPU improves its speed of processing, addressing and executing instructions compared to the conventional 8-bit versions.

This section describes the CPU functions available to the programmer.

3.1.1 Memory map

The TMP90C840 supports a program memory of up to 64K bytes and a data memory of maximum 1M bytes.

The program memory may be assigned to the address space from OOOOOH to OFFFFH, while the data memory can be allocated to any address from OOOOOH to FFFFFH.

(1) Internal ROM

The TMP90C840 internally contains an 8K-byte ROM. The address space from OOOOH to lFFFH is provided to the ROM. The CPU starts executing a program from OOOOH by resetting. The addresses OOlOH to 007FH in this internal ROM area are used for the entry area for the interrupt processing.

(2) Internal RAM

The TMP90C840 also contains a 256 byte RAM, which is allocated to the address space from FECOH to FFBFH. The CPU allows the access to a certain RAM area (FFOOH to FFBFH, 192 bytes) by a short operation code (opcode) in a "direct addressing mode".

The addresses from FFlOH to FF7FH in this RAM area can be used as parameter area for micro DMA processing (and for any other purposes when the micro DMA function is not used).

(3) Internal I/O

The TMP90C840 provides a 48-byte address space as an internal I/O area, whose addresses range from FFCOH to FFEFH. This I/O area can be accessed by the CPU using a short opcode in the "direct addressing mode".

Fig. 3.1 (1) is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

3. OPERATION

This chapter describes the functions and the basic
TMP90C840 in every block.

3.1 CPU

The TMP90C840 incorporates a high-performance 8-bi
improves its speed of processing, addressing and exe
compared to the conventional 8-bit versions.
This section describes the CPU functions available to

3.1.1 Memory map

The TMP90C840 supports a program memory of up to 6
memory of maximum 1M bytes.
The program memory may be assigned to the address s
OFFFFH, while the data memory can be allocated t
OOOOOH to FFFFFH.

(1) Internal ROM

The TMP90C840 internally contains an 8K-byte ROM.
from 0000H to 1FFFH is provided to the ROM. The C
a program from 0000H by resetting.
The addresses 0010H to 007FH in this internal ROM
the entry area for the interrupt processing.

(2) Internal RAM

The TMP90C840 also contains a 256 byte RAM, which
address space from FECOH to FFBFH. The CPU allo
certain RAM area (FF00H to FFBFH, 192 bytes) by a s
(opcode) in a "direct addressing mode".
The addresses from FF10H to FF7FH in this RAM a
parameter area for micro DMA processing (and for
when the micro DMA function is not used).

(3) Internal I/O

The TMP90C840 provides a 48-byte CPU address space
area, whose addresses range from FFCOH to FFEFH.
accessed by the CPU using a short opcode in the

Table of Contents

Previous Page
Next Page

Quick Links:

Related Manuals for Toshiba TLCS-90 Series

Microcontrollers Toshiba H1 Series Data Book

32bit micro controller tlcs-900/h1 series (751 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (544 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (652 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Data Book

32bit micro controller (495 pages)
Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (68 pages)
Microcontrollers Toshiba TMP96C141AF Manual

Cmos 16-bit microcontroller (178 pages)
Microcontrollers Toshiba TLCS-870/C Series Manual

8 bit microcontroller (191 pages)
Microcontrollers Toshiba TLCS-870/C Series Manual

8 bit microcontroller (205 pages)
Microcontrollers Toshiba TLCS-870/C1 Series Manual

8 bit microcontroller (408 pages)
Microcontrollers Toshiba TLCS-900/L1 Series Manual

Original cmos 16-bit microcontroller (261 pages)
Microcontrollers Toshiba TLCS-900/L1 Series Manual

Original cmos 16-bit microcontroller (204 pages)
Microcontrollers Toshiba TXZ Family Reference Manual

32-bit risc microcontroller txz family reference manual comparator (comp-b) (15 pages)
Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller. can controller (can-a) (54 pages)
Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller, serial peripheral inteface tspi-b (67 pages)
Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller (17 pages)
Microcontrollers TOSHIBA TXZ SERIES Reference Manual

Oscillation frequency detector (20 pages)

Related Content for Toshiba TLCS-90 Series

TXZ+ Series Elosc Setting (No Operation Of External Low Speed Oscillator → Operation)
Toshiba TXZ+ Series

TXZ+ Series Clock Control And Operation Mode
Toshiba TXZ+ Series

TLCS-900/L1 Series Operation
Toshiba TLCS-900/L1 Series

TLCS-870/C Series Operation Mode Control Circuit
Toshiba TLCS-870/C Series

TX03 Series Reset Operation
Toshiba TX03 Series

TLCS-900/H1 Series Operation
Toshiba TLCS-900/H1 Series

TLCS-870/C1 Series Warm-Up Counter Operation When The Oscillation Is Enabled By The Hardware
Toshiba TLCS-870/C1 Series

TXZ Series Operation Description

This manual is also suitable for:

Tlcs-48 seriesTmp90c840nTmp80c840fTmp90c840eTmp8048aTmp8035a ... Show all