Toshiba TLCS-900/L1 Series Manual

Original cmos 16-bit microcontroller

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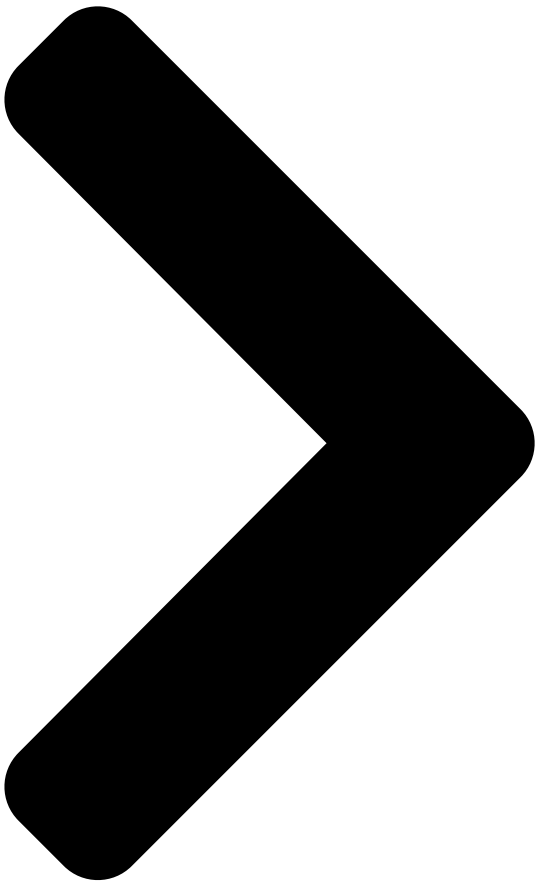
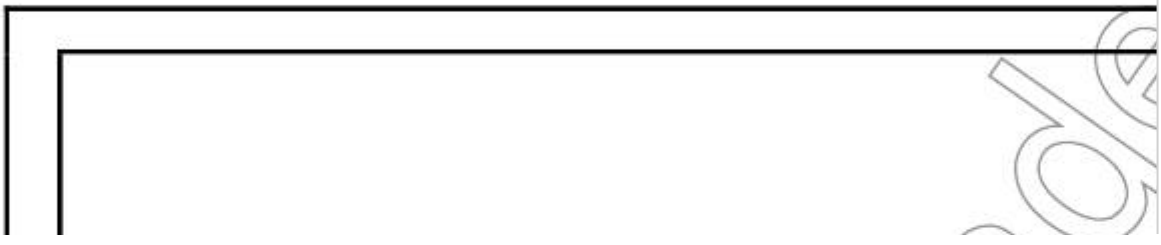


TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91C824FG

Semiconductor Company



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Summary of Contents for Toshiba TLCS-900/L1 Series

Page 1 TOSHIBA Original CMOS 16-Bit Microcontroller TLCS-900/L1 Series TMP91C824FG Semiconductor Company...

Page 2 Preface Thank you very much for making use of Toshiba microcomputer LSIs. Before use this LSI, refer the section, “Points of Note and Restrictions”. Especially, take care below cautions. **CAUTION** How to release the HALT mode Usually, interrupts can release all halts status. However, the interrupts = (...

Page 3: Outline And Features

It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

Page 4 = 2.7 V to 3.6 V (fc max = 33 MHz) • = 1.8 V to 3.6 V (fc max = 10 MHz) (19) Package • 100-pin QFP: LQFP100-P-1414-0.50F • Chip form supply also available. For details, contact your local Toshiba sales representative. 91C824-2 2008-02-20...

Page 5 TMP91C824 (P83) DVCC [2] ADTRG AN0 to AN7 (P80 to P87) DVSS [2] 10-bit 8-channel converter AVCC, AVSS H-OSC VREFH, VREFL EMU0 Clock gear, Clock doubler TXD0 (PC0) EMU1 32 bits SIO/UART/IrDA RXD0 (PC1) (SIO0) L-OSC SCLK0/ (PC2) TXD1 (PC3) SCOUT (PD5) SIO/UART RXD1 (PC4)

Page 6: Pin Assignment Diagram

TMP91C824 Pin Assignment and Functions The assignment of input/output pins for the TMP91C824, their names and functions are as follows: Pin Assignment Diagram Figure 2.1 shows the pin assignment of the TMP91C824FG. VREFL AVSS AVCC P80/AN0 P81/AN1 P20/A16 P82/AN2 P83/AN3/ ADTRG P21/A17 P84/AN4...

Page 7: Pad Layout

TMP91C824 Pad Layout (Chip size 4.37 mm × 4.37 mm) Unit: µm Name X Point Y Point Name X Point Y Point Name X Point Y Point −2050 −140 −2050 1 VREFL 1721 2045 −2050 −14 −2050 2 AVSS 1596 2045 1075 −2050...

Page 8: Pin Names And Functions

TMP91C824 Pin Names and Functions The names of the input/output pins and their functions are described below. Table 2.3.1 Pin Names and Functions (1/3) Number Pin Name Functions of Pins D0 to D7 Data (Lower): Bits 0 to 7 of data bus P10 to P17 Port 1: I/O port that allows I/O to be selected at the bit level (when used to the external 8-bit bus)

Page 9 TMP91C824 Table 2.3.2 Pin Names and Functions (2/3) Number Pin Name Functions of Pins Port 70: I/O port Serial bus interface clock I/O data at SIO mode OPTRX0 Input Serial 0 receive data Port 71: I/O port Output Serial bus interface send data at SIO mode Serial bus interface send/receive data at I C bus mode Open-drain output mode by programmable (with pull up)

Page 10 TMP91C824 Table 2.3.3 Pin Names and Functions (3/3) Number Pin Name Functions of Pins Port C2: I/O port SCLK0 Serial 0 clock CTS0 Input Serial data send enable 0 (Clear to send) Port C3: I/O port TXD1 Output Serial 1 send data Open-drain output pin by programmable Port C4: I/O port RXD1...

Page 11: Operation

TMP91C824 Operation This following describes block by block the functions and operation of the TMP91C824. Notes and restrictions for eatch book are outlined in 6 “Precautions and Restrictions” at the end of this manual. The TMP91C824 incorporates a high-performance 16-bit CPU (the 900/L1 CPU). For CPU operation, see the TLCS-900/L1 CPU.

Page 12 TMP91C824 Read Write Figure 3.1.1 TMP91C824 Reset Timing Chart 91C824-10 2008-02-20...

Page 13: Memory Map

16-Mbyte area (−R) (R+) (R + R8/16) (R + d8/16) (nnn) FFFF00H Vector table (256 bytes) FFFFFFH Internal area) Figure 3.2.1 Memory Map Note: Address 000FE0H to 00FFFH is assigned for the TOSHIBA reserve area, user can’t use. 91C824-11 2008-02-20...

Page 14 TMP91C824 Triple Clock Function and Standby Function TMP91C824 contains (1) clock gear, (2) clock doubler (DFM), (3) standby controller and (4) noise-reduction circuit. It is used for low-power and low-noise systems. This chapter is organized as follows: 3.3.1 Block Diagram of System Clock 3.3.2 SFR 3.3.3 System Clock Controller 3.3.4 Prescaler Clock

Controller...

Page 15 TMP91C824 The clock operating modes are as follows: (a) Single clock mode (X1, X2 pins only), (b) Dual clock mode (X1, X2, XT1 and XT2 pins) and (c) Triple clock mode (The X1, X2, XT1 and XT2 pins and DFM). Figure 3.3.1 shows a transition figure.

Page 16 TMP91C824 3.3.1 Block Diagram of System Clock SYSCR0<WUEF> SYSCR2<WUPTM1:0> DFMCR0<ACT1:0, DLUPTM> SYSCR0 Warm-up timer (High-/low-frequency φT <PRCK1:0> oscillator), Lockup timer (DFM) φT0 fc/16 ÷2 ÷4 SYSCR0 <XTEN, RXTEN> Low-frequency ÷2 oscillator fc/2 × 4 OSCH fc/4 SYSCR0 fc/8 SYSCR1<SYSCK> <XEN, RXEN> Selector fc/16 Clock doubler...

Page 17 TMP91C824 3.3.2 Bit symbol SYSCR0 XTEN RXEN RXTEN RSYSCK WUEF PRCK1 PRCK0 Read/Write (00E0H) After reset Function Warm-up timer High- Low- High- Low- Selects clock Select prescaler clock 0: Write 00: f (Note 2) frequency frequency frequency frequency after release Don’t care oscillator (fc) oscillator (fs)

Page 18 TMP91C824 Bit symbol DFMCR0 ACT1 ACT0 DLUPFG DLUPTM (00E8H) Read/Write After reset Function DFM LUP select f Lockup Lockup time status flag 0: 2 STOP STOP f OSCH OSCH 0: LUP end 1: 2 OSCH OSCH 1: LUP not STOP f STOP f OSCH Bit symbol...

Page 19 TMP91C824 − − − − EMCCR0 Bit symbol PROTECT EXTIN DRVOSCH DRVOSCL Read/Write (00E3H) After reset Function Protect flag Always Always Always Always 1: External fc oscillator fs oscillator 0: OFF write 0 write 1 write 0 write 0 clock driver ability driver ability 1: ON...

Page 20 TMP91C824 3.3.3 System Clock Controller The system clock controller generates the system clock signal (f) for the CPU core and internal I/O. It contains two oscillation circuits and a clock gear circuit for high- frequency (fc) operation. The register SYSCR1<SYSCK> changes the system clock to either fc or fs, SYSCR0<XEN>...

Page 21 TMP91C824 Example 1: Setting the clock Changing from high frequency (fc) to low frequency (fs). SYSCR0 00E0H SYSCR1 00E1H SYSCR2 00E2H WDMOD 005CH (SYSCR2), X−11−− − −B ; Sets warm-up time to 2 /fs. 6, (SYSCR0) ; Enables low-frequency oscillation. 2, (SYSCR0) ;...

Page 22 TMP91C824 Example 2: Setting the clock Changing from low frequency (fs) to high frequency (fc). SYSCR0 00E0H SYSCR1 00E1H SYSCR2 00E2H (SYSCR2), X−10− − − −B ; Sets warm-up time to 214/fc. 7, (SYSCR0) ; Enables high-frequency oscillation. 2, (SYSCR0) ;...

Page 23 TMP91C824 (2) Clock gear controller When the high-frequency clock fc is selected by setting SYSCR1<SYSCK> = 0, f is set according to the contents of the clock gear select register SYSCR1<GEAR0:2> to either fc, fc/2, fc/4, fc/8 or fc/16. Using the clock gear to select a lower value of f reduces power consumption.

Page 24 TMP91C824 3.3.4 Prescaler Clock Controller For the internal I/O (TMRA01 to TMRA23, SIO0 to SIO1) there is a prescaler which can divide the clock. The φT0 clock input to the prescaler is either the clock f divided by 4 or the clock fc/16 divided by 4.

Page 25: Start Up Control

TMP91C824 Limitation point on the use of DFM 1. it’s prohibited to execute DFM enable/disable control in the SLOW mode (fs). You should control DFM in the NORMAL mode. 2. If you stop DFM operation during using DFM (DFMCR0<ACT1:0> = “10”), you shouldn’t execute the commands that change the clock f to f and stop the...

Page 26 TMP91C824 Change/stop control (OK) DFM use mode (f) → High-frequency oscillator operation mode (f) → OSCH DFM stop → Low-frequency oscillator operation mode (fs) → High-frequency oscillator stop (DFMCR0), 11------B Change the system clock f to f OSCH (DFMCR0), 00------B DFM stop Change the system clock f...

Page 27 TMP91C824 3.3.6 Noise Reduction Circuits Noise reduction circuits are built in, allowing implementation of the following features. (1) Reduced drivability for high-frequency oscillator (2) Reduced drivability for low-frequency oscillator (3) Single drive for high-frequency oscillator (4) SFR protection of register contents (5) ROM protection of register contents (1)

Reduced drivability for high-frequency oscillator (Purpose)

Page 28 TMP91C824 (2) Reduced drivability for low-frequency oscillator (Purpose) Reduces noise and power for oscillator when a resonator is used. (Block diagram) XT1 pin Enable oscillation Resonator EMCCR0<DRVOSCL> XT2 pin (Setting method) The drivability of the oscillator is reduced by writing 0 to the EMCCR0 <DRVOSCL>...

Page 29 TMP91C824 (4) Runaway provision with SFR protection register (Purpose) Provision in runaway of program by noise mixing. Write operation to specified SFR is prohibited so that provision program in runaway prevents that it is it in the state which is fetch impossibility by stopping of clock, memory control register (CS/WAIT controller, MMU) is changed.

Page 30 TMP91C824 (5) Runaway provision with ROM protection register (Purpose) Provision in runaway of program by noise mixing. (Operation explanation) When write operation was executed for external three kinds of ROM by runaway of program, INTP1 is occurred and detects runaway function. Three kinds of ROM is fixed as for flash ROM (Option program ROM), data ROM, program ROM are as follows on the logical address memory map.

Page 31 TMP91C824 3.3.7 Standby Controller (1) HALT modes When the HALT instruction is executed, the operating mode switches to IDLE2, IDLE1 or STOP mode, depending on the contents of the SYSCR2<HALTM1:0> register. The subsequent actions performed in each mode are as follows: IDLE2: Only the CPU halts.

Page 32 TMP91C824 (2) How to release the HALT mode These halt states can be released by resetting or requesting an interrupt. The HALT release sources are determined by the combination between the states of interrupt mask register <IFF2:0> and the HALT modes. The details for releasing the halt status are shown in Table 3.3.4.

Page 33 TMP91C824 Table 3.3.4 Source of Halt State Clearance and Halt Clearance Operation Interrupt Enabled Interrupt Disabled Status of Received Interrupt (Interrupt level) ≥ (Interrupt mask) (Interrupt level) < (Interrupt mask) HALT Mode IDLE2 IDLE1 STOP IDLE2 IDLE1 STOP ♦ ♦ ♦...

Page 34 TMP91C824 (3) Operation IDLE2 mode In IDLE2 mode only specific internal I/O operations, as designated by the IDLE2 setting register, can take place. Instruction execution by the CPU stops. Figure 3.3.6 illustrates an example of the timing for clearance of the IDLE2 mode halt state by an interrupt.

Page 35 TMP91C824 STOP mode When STOP mode is selected, all internal circuits stop, including the internal oscillator pin status in STOP mode depends on the settings in the SYSCR2<DRVE> register. Table 3.3.6, Table 3.3.7 summarizes the state of these pins in STOP mode. After STOP mode has been cleared system clock output starts when the warm-up time has elapsed, in order to allow oscillation to stabilize.

Page 36 TMP91C824 Example: The STOP mode is entered when the low-frequency operates, and high-frequency operates after releasing due to NMI. Address SYSCR0 00E0H SYSCR1 00E1H SYSCR2 00E2H = fs/2 8FFDH (SYSCR1), 08H 9000H (SYSCR2), X−1001−1B ; Sets warm-up time to 2 OSCH (SYSCR0), 011000 −...

Page 37 TMP91C824 Table 3.3.6 Input Buffer State Table Input Buffer State When the CPU is In HALT mode(IDLE1/STOP) In HALT mode(IDLE2) Input operating Condition A (Note) Condition B (Note) Port Function During When When Name When Used When When When When Used When Name Reset...

Page 38 TMP91C824 Table 3.3.7 Output buffer State Table Output Buffer State When the CPU is In HALT mode (IDLE1/STOP) In HALT mode(IDLE2) Output Operating Condition A (Note) Condition B (Note) Port Function During When When When When When When When When Name Name Reset...

Page 39 TMP91C824 Interrupts Interrupts are controlled by the CPU interrupt mask register SR<IFF2:0> and by the built- in interrupt controller. The TMP91C824 has a total of 37 interrupts divided into the following five types: • Interrupts generated by CPU: 9 sources (Software interrupts, illegal instruction interrupt) •...

Page 40 TMP91C824 Interrupt processing Micro DMA soft start request Interrupt specified by micro DMA start vector? Clear interrupt request flag Data transfer by Interrupt vector value V micro DMA read Interrupt request F/F clear General-purpose PUSH Count ← Count − 1 Micro DMA processing interrupt PUSH...

Page 41 TMP91C824 3.4.1 General-purpose Interrupt Processing When the CPU accepts an interrupt, it usually performs the following sequence of operations. That is also the same as TLCS-900/L and TLCS-900/H. (1) The CPU reads the interrupt vector from the interrupt controller. If the same level interrupts occur simultaneously, the interrupt controller generates an interrupt vector in accordance with the default priority and clears the interrupt request.

Page 42 TMP91C824 Table 3.4.1 TMP91C824 Interrupt Vectors Table Vector Default Interrupt Source and Source of Micro DMA Vector Micro DMA Type Reference Priority Request Value (V) Start Vector Address − Reset or “SWI 0” instruction 0000H FFFF00H − “SWI 1” instruction 0004H FFFF04H −...

Page 43 TMP91C824 3.4.2 Micro DMA Processing In addition to general-purpose interrupt processing, the TMP91C824 supprots a micro DMA function. Interrupt requests set by micro DMA perform micro DMA processing at the highest priority level (Level 6) among maskable interrupts, regardless of the priority level of the particular interrupt source.

Page 44 TMP91C824 If a micro DMA request is set for more than one channel at the same time, the priority is not based on the interrupt priority level but on the channel number. The smaller channel number has the higher priority (Channel 0 (High) > Channel 3 (Low)). While the register for setting the transfer source/transfer destination addresses is a 32-bit control register, this register can only effectively output 24-bit addresses.

Page 45 TMP91C824 (2) Soft start function In addition to starting the micro DMA function by interrupts, TMP91C824 includes a micro DMA software start function that starts micro DMA on the generation of the write cycle to the DMAR register. Writing “1” to each bit of DMAR register causes micro DMA once (If write “0” to each bit, micro DMA doesn’t operate).

Page 46 TMP91C824 (4) Detailed description of the transfer mode register 8 bits Note: When setting a value in this register, write 0 to the upper 3 bits. DMAM0 to Mode DMAM3 Minimum Number of Number of Mode Description Execution Time Transfer Bytes Execution States at fc = 33 MHz Byte transfer...

Page 47 TMP91C824 3.4.3 Interrupt Controller Operation The block diagram in Figure 3.4.3 shows the interrupt circuits. The left-hand side of the diagram shows the interrupt controller circuit. The right-hand side shows the CPU interrupt request signal circuit and the halt release circuit. For each of the 36 interrupt channels there is an interrupt request flag (Consisting of a flip-flop), an interrupt priority setting register and a micro DMA start vector register.

Page 48 TMP91C824 Figure 3.4.3 Block Diagram of Interrupt Controller 91C824-46 2008-02-20...

Page 49 TMP91C824 (1) Interrupt level setting registers Name Address Symbol INTAD INT0 INT0 & IADC IADM2 IADM1 IADM0 I0M2 I0M1 I0M0 INTE0AD INTAD enable INT2 INT1 INT1 & I2M2 I2M1 I2M0 I1M2 I1M1 I1M0 INTE12 INT2 enable INTALM4 INT3 INT3 & IA4C IA4M2 IA4M1...

Page 50 TMP91C824 Name Address Symbol INTTX0 INTRX0 Interrupt ITX0C ITX0M2 ITX0M1 ITX0M0 IRX0C IRX0M2 IRX0M1 IRX0M0 INTES0 Enable serial 0 INTTX1 INTRX1 INTRX1 & ITX1C ITX1M2 ITX1M1 ITX1M0 IRX1C IRX1M2 IRX1M1 IRX1M0 INTES1 INTTX1 enable INTSBI ISBIC ISBIM2 ISBIM1 ISBIM0 INTESBI INTES2 enable INTTC1...

Page 51: External Interrupt Control

TMP91C824 (2) External interrupt control Name Address Symbol − − I3EDGE I2EDGE I1EDGE I0EDGE I0LE NMIREE Interrupt Always Always INT3EDGE INT2EDGE INT1EDGE INT0EDGE INT0 mode 1: Operates input IIMC write 0 write 0 0: Rising 0: Rising 0: Rising 0: Rising 0: Edge even on mode...

Page 52 TMP91C824 Symbol Name Address DMA0V5 DMA0V4 DMA0V3 DMA0V2 DMA0V1 DMA0V0 DMA0 DMA0V start vector DMA0 start vector DMA1V5 DMA1V4 DMA1V3 DMA1V2 DMA1V1 DMA1V0 DMA1 DMA1V start vector DMA1 start vector DMA2V5 DMA2V4 DMA2V3

DMA2V2 DMA2V1 DMA2V0 DMA2 DMA2V start vector DMA2 start vector DMA3V5 DMA3V4...

Page 53 TMP91C824 (6) Attention point The instruction execution unit and the bus interface unit of this CPU operate independently. Therefore, immediately before an interrupt is generated, if the CPU fetches an instruction that clears the corresponding interrupt request flag, the CPU may execute the instruction that clears the interrupt request flag (Note) between accepting and reading the interrupt vector.

Page 54: Port Functions

TMP91C824 Port Functions The TMP91C824 features 56-bit settings which relate to the various I/O ports. As well as general-purpose I/O port functionality, the port pins also have I/O functions which relate to the built-in CPU and internal I/Os. Table 3.5.1 lists the functions of each port pin.

Page 55 TMP91C824 Table 3.5.2 I/O Registers and Specifications (1/2) I/O Register Port Pin Name Specification PnCR PnFC PnFC2 Port 1 P10 to P17 Input port (Note 1) None Output port D8 to D15 bus Port 2 P20 to P27 Output port None A16 to A23 output Port 5...

Page 56 TMP91C824 Table 3.5.3 I/O Registers and Specifications (2/2) I/O Register Port Pin Name Specification PnCR PnFC PnFC2 Port 8 P80 to P87 Input port None AN0 to 7 input (Note 4) input (Note 5) ADTRG Port B PB0 to PB6 Input port Output port TA0IN input...

Page 57 TMP91C824 Note about bus release and programmable pull-up I/O port pins = 0), the output buffers for D0 to D15, A0 to When the bus is released (e.g., when BUSAK A23, and the control signals (, EA24, EA25, CS2A) are off and are set to high impedance.

Page 58 TMP91C824 3.5.1 Port 1 (P10 to P17) Port 1 is an 8-bit general-purpose I/O port. Each bit can be set individually for input or output using the control register P1CR. Resetting the control register P1CR to 0 and sets port 1 to input mode. In addition to functioning as a general-purpose I/O port, port 1 can also function as an address data bus (D8 to D15).

Page 59 TMP91C824 3.5.2 Port 2 (P20 to P27) Port 2 is an 8-bit output port. In addition to functioning as a output port, port 2 can also function as an address bus (A16 to A23). Each bit can be set individually for address bus using the function register P2FC. Resetting sets all bits of the function register P2FC to 1 and sets port 2 to address bus.

Page 60 TMP91C824 Port 1 Register Bit symbol (0000H) (0001H) Read/Write After reset Data from external port (Output latch register is cleared to 0.) Port 1 Control Register P1CR Bit symbol P17C P16C P15C P14C P13C P12C P11C P10C (0004H) Read/Write After reset Function 0: Input 1: Output...

Page 61 TMP91C824 3.5.3 Port 5 (P54 to P56) Port 5 is an 3-bit general-purpose I/O port. I/O is set using control register P5CR and P5FC. Resetting resets all bits of the output latch P5 to 1, the control register P5CR and the function register P5FC to 0 and sets P54 to P56 to input mode with pull-up resistor.

Page 62 TMP91C824 Reset Direction control (on bit basis) P-ch (Programmable pull up) P5CR write Output P56 (WAIT latch Output buffer P5 write P5 read Internal WAIT Reset Direction control (on bit basis) P5CR write Function control (on bit basis) P-ch (Programmable pull up) P5FC write Output P54 (...

Page 63 TMP91C824 Port 5 Register Bit symbol (000DH) Read/Write After reset Data from external port (Output latch register is set to “1”.) 0(Output latch register) : Pull-up resistor OFF Function 1(Output latch register) : Pull-up resistor ON Port 5 Control Register P5CR Bit symbol P56C...

Page 64 TMP91C824 3.5.4 Port 6 (P60 to P67) Port 60 to 67 are 8-bit output ports. Resetting sets output latch of P62 to 0 and output latches of P60 to P61, P63 to P67 to 1. Port 6 also function as chip-select output ( ), extend address output (EA24).

Page 65 TMP91C824 Port 6 Register Bit symbol (0012H) Read/Write After reset Port 6 Function Register − − Bit symbol P65F P64F P63F P62F P61F P60F P6FC (0015H) Read/Write After reset Function Always write 0 0:Port 0: Port 0: Port 0: Port 0: Port 0: Port 1:EA25...

Page 66 TMP91C824 3.5.5 Port 7 (P70 to P72) Port 7 is a 3-bit general-purpose I/O port. I/O can be set on bit basis using the control register. Resetting sets port 7 to input port and all bits of output latch to 1. In addition to functioning as a general-purpose I/O port, port 7 also functions as follows.

Page 67 TMP91C824 (2) Port 71 (SO/SDA/OPTTX0) Port 71 is a general-purpose I/O port. It is also used as SDA (Data input for I mode), SO (Data output for SIO mode) for serial bus interface and OPTTX0 (Transmit output for IrDA mode of SIO0). Used as OPTTX0, it is possible to logical invert by P7<P71>...

Page 68 TMP91C824 (3) Port 72 (SI/SCL) Port 72 is a general-purpose I/O port. It is also used as SI (Data input for SIO mode), SCL (Clock input/output for I C mode) for serial bus interface and input for release hard protect. Reset Direction control...

Page 69 TMP91C824 Port 7 Register Bit symbol (0013H) Read/Write After reset Data from external port (Output latch register is set to “1”.) Function 0(Output latch register) : Pull-up resistor ON – 1(Output latch register) : Pull-up resistor OFF Port 7 Control Register Bit symbol P72C P71C...

Page 70 TMP91C824 3.5.6 Port 8 (P80 to P87) Port 8 is an 8-bit input port and can also be used as the analog input pins for the internal AD converter. P83 can also be used as ADTRG pin for the AD converter. Port 8 P80 to P87 Port 8 read...

Page 71 TMP91C824 3.5.7 Port B (PB0 to PB6) Port B0 to PB6 is a 7-bit general-purpose I/O port. Each bit can be set individually for input or output. Resetting sets port B to be an input port. In addition to functioning as a general-purpose I/O port, port B0 has clock input terminal TA0IN of 8-bit timer 0, and port B1, B2 each has facility of 8-bit timer listing TA1OUT, TA3OUT terminal.

Page 72 TMP91C824 (2) PB3 (INT0), PB4 (INT1) to PB6 (INT3) Reset Direction control (on bits basis) PBCR write Function control (on bits basis) PBFC write Output latch PB3 (INT0) PB write Selector PB read Level/edge select & INT0 Rising/falling select IIMC<I0LE, I0EDGE> Figure 3.5.16 Port B3 Reset Direction control...

Page 73 TMP91C824 Port B Register Bit symbol (0022H) Read/Write After reset Data from external port (Output latch register is set to “1”.) Port B Control Register PBCR Bit symbol PB6C PB5C PB4C PB3C PB2C PB1C PB0C (0024H) Read/Write After reset Function 0: Input 1: Output Port B Function Register...

Page 74 TMP91C824 3.5.8 Port C (PC0 to PC5) Port C0 to C5 are 6-bit general-purpose I/O ports. Each bit can be set individually for input or output. Resetting sets PC0 to PC5 to be an input ports. It also sets all bits of the output latch register to 1.

Page 75 TMP91C824 (2) Port C1, C4 (RXD0, RXD1) Port C1 and C4 are I/O port pins and can also is used as RXD input for the serial channels. In case of use RXD0/RXD1, it is possible to logical invert by setting the register PC<PC1, 4>.

Page 76 TMP91C824 Port C Register Bit symbol (0023H) Read/Write After reset Data from external port (Output latch register is set to “1”.) Port C Control Register Bit symbol PC5C PC4C PC3C PC2C PC1C PC0C PCCR Read/Write (0026H) After reset Function 0: Input 1: Output Port C Functon Register Bit symbol...

Page 77 TMP91C824 3.5.9 Port D (PD0 to PD7) Port D is an 8-bit output port. Resetting sets the output latch PD to 1, and PD5 to PD7 pin output 1. In addition to functioning as output port, port D also function as output pin for output pin for internal clock (SCOUT), output pin for RTC alarm ( ) and output pin for ALARM...

Page 78 TMP91C824 Reset Function control (on bit basis) PDFC write Output latch PD6 (ALARM Selector MLDALM PD write PD read MLDALM Selector ALARM Figure 3.5.25 Port D Port D Register Bit symbol (0029H) Read/Write After reset Port D Function Register Bit symbol PD7F PD6F...

Page 79 TMP91C824 3.5.10 Port Z (PZ2 to PZ3) Port Z is the 2-bit general-purpose I/O port. I/O is set using control register PZCR and PZFC. Resetting resets all bits of the output latch PZ to

1. In addition to functioning as a general-purpose I/O port, port Z also functions as output for the CPU’s control/status signal.

Page 80 TMP91C824 Reset Direction control (on bit basis) PZCR write Function conrtol (on bit basis) P-ch (Programmable pull up) PZFC write Output PZ2 (latch Output buffer PZ write PZ read Reset Direction control (on bit basis) PZCR write Function conrtol (on bit basis) P-ch (Programmable pull up) PZFC write...

Page 81 TMP91C824 Port Z Register Bit symbol (007DH) Read/Write After reset Data from external port (Output latch register is set to “1”.) Function 0(Output latch register) : Pull-up resistor OFF 1(Output latch register) : Pull-up resistor ON Port Z Control Register Bit symbol PZ3C PZ2C...

Page 82: Chip Select/Wait Controller

TMP91C824 Chip Select/Wait Controller On the TM91C824, four user-specifiable address areas (CS0 to CS3) can be set. The data bus width and the number of waits can be set independently for each address area (CS0 to CS3 and others). The pins (which can also function as port pins P60 to P63) are the respective output pins for the areas CS0 to CS3.

Page 83 TMP91C824 (1) Memory start address registers Figure 3.6.1 shows the memory start address registers. The memory start address registers MSAR0 to MSAR3 set the start addresses for the CS0 to CS3 areas. Set the upper 8 bits (A23 to A16) of the start address in <S23:16>. The lower 16 bits of the start address (A15 to A0) are permanently set to 0.

Page 84 TMP91C824 (2) Memory address mask registers Figure 3.6.3 shows the memory address mask registers. Memory address mask registers MAMR0 to MAMR3 are used to set the size of the CS0 to CS3 areas by specifying a mask for each bit of the start address set in memory start address registers MAMR0 to MAMR3.

Page 85 TMP91C824 (3) Setting memory start addresses and address areas Figure 3.6.4 show an example of specifying a 64-Kbyte address area starting from 010000H using the CS0 areas. Set 01H in memory start address register MSAR0<S23:16> (Corresponding to the upper 8 bits of the start address). Next, calculate the difference between the start address and the anticipated end address (01FFFFH).

Page 86 TMP91C824 (4) Address area size specification Table 3.6.1 shows the relationship between CS area and area size. “Δ” indicates areas that cannot be set by memory start address register and address mask register combinations. When setting an area size using a combination indicated by “Δ”, set the start address mask register in the desired steps starting from 000000H.

Page 87 TMP91C824 B0CS Bit symbol B0OM1 B0OM0 B0BUS B0W2 B0W1 B0W0 (00C0H) Read/Write After reset Read- Function 0: Disable Chip select output Data bus Number of waits modify- 1: Enable waveform selection width 000: 2 waits 100: Reserved write instructions 00: For ROM/SRAM 0: 16 bits 001: 1 wait 101: 3 waits...

Page 88 TMP91C824 (1) Master enable bits Bit 7 (<B0E>, <B1E>, <B2E> or <B3E>) of a chip select/wait control register is the master bit which is used to enable or disable settings for the corresponding address area. Writing 1 to this bit enables the settings. Reset disables (Sets to 0) <B0E>, <B1E>...

Page 89 TMP91C824 (3) Wait control Bits 0 to 2 (<B0W0:2>, <B1W0:2>, <B2W0:2>, <B3W0:2>, <BEXW0:2>) of a chip select/wait control register specify the number of waits that are to be inserted when the corresponding memory area is accessed. The following types of wait operation can be specified using these bits. Bit settings other than those listed in the table should not be made.

Page 90 TMP91C824 (6) Procedure for setting chip select/wait control When using the chip select/wait control function, set the registers in the following order: Set the memory start address registers MSAR0 to MSAR3. Set the start addresses for CS0 to CS3. Set the memory address mask registers MAMR0 to MAMR3. Set the sizes of CS0 to CS3.

Page 91 TMP91C824 3.6.3 Connecting External Memory Figure 3.6.6 shows an example of how to connect external memory to the TMP91C824. In this example the ROM is connected

using a 16-bit bus. The RAM and I/O are connected using an 8-bit bus. TMP91C824 Address bus Upper byte...

Page 92: 8-Bit Timers (Tmra)

TMP91C824 8-Bit Timers (TMRA) The TMP91C824 features 4 channel (TMRA0 to TMRA3) built-in 8-bit timers. These timers are paired into 2 modules: TMRA01 and TMRA23. Each module consists of 2 channels and can operate in any of the following 4 operating modes. •...

Page 93 TMP91C824 3.7.1 Block Diagrams Figure 3.7.1 TMRA01 Block Diagram 91C824-91 2008-02-20...

Page 94 TMP91C824 Figure 3.7.2 TMRA23 Block Diagram 91C824-92 2008-02-20...

Page 95 TMP91C824 3.7.2 Operation of Each Circuit (1) Prescalers A 9-bit prescaler generates the input clock to TMRA01. The φT0 as the input clock to prescaler is a clock divided by 4 which selected using the prescaler clock selection register SYSCR0<PRCK1:0>. The prescaler's operation can be controlled using TA01RUN<TA01PRUN>...

Page 96 TMP91C824 (3) Timer registers (TA0REG and TA1REG) These are 8-bit registers which can be used to set a time interval. When the value set in the timer register TA0REG or TA1REG matches the value in the corresponding up counter, the comparator match detect signal goes active. If the value set in the timer register is 00H, the signal goes active when the up counter overflows.

Page 97 TMP91C824 (4) Comparator (CP0) The comparator compares the value in an up counter with the value set in a timer register. If they match, the up counter is cleared to zero and an interrupt signal (INTTA0 or INTTA1) is generated. If timer flip-flop inversion is enabled, the timer flip-flop is inverted at the same time.

Page 98 TMP91C824 3.7.3 SFRs TMRA01 Run Register Bit symbol TA0RDE I2TA01 TA1RUN TA0RUN TA01RUN TA01PRUN (0100H) Read/Write After reset Function Double IDLE2 8-bit timer run/stop control buffer 0: Stop 0: Stop and clear 0: Disable 1: Operate 1: Run (Count up) 1: Enable TA0REG double buffer control Timer run/stop control...

Page 99 TMP91C824 TMRA01 Mode Register TA01MOD Bit symbol TA01M1 TA01M0 PWM01 PWM00 TA1CLK1 TA1CLK0 TA0CLK1 TA0CLK0 (0104H) Read/Write After reset Function Operation mode PWM cycle Source clock for TMRA1 Source clock for TMRA0 00: 8-bit timer mode 00: Reserved 00: TA0TRG 00: TA0IN pin 01: φT1 01: φT1...

Page 100 TMP91C824 TMRA23 Mode Register TA23MOD Bit symbol TA23M1 TA23M0 PWM21 PWM20 TA3CLK1 TA3CLK0 TA2CLK1 TA2CLK0 (010CH) Read/Write After reset Function Operation mode PWM cycle TMRA3 clock for TMRA3 TMRA2 clock for TMRA2 00: 8-bit timer mode 00: Reserved 00: TA2TRG 00: Reserved 01: φT1 01: φT1...

Page 101 TMP91C824 TMRA1 Flip-Flop Control Register TA1FFCR Bit symbol TA1FFC1 TA1FFC0 TA1FFIE TA1FFIS (0105H) Read/Write After reset Read- Function 00: Invert TA1FF TA1FF TA1FF modify-write 01: Set TA1FF control for inversion instructions 10: Clear TA1FF inversion select prohibited. 11: Don't care 0: Disable 0: TMRA0 1: Enable...

Page 102 TMP91C824 TMRA3 Flip-Flop Control Register TA3FFCR Bit symbol TA3FFC1 TA3FFC0 TA3FFIE TA3FFIS (010DH) Read/Write After reset Read- modify-write Function 00: Invert TA3FF TA3FF TA3FF instructions 01: Set TA3FF control for inversion 10: Clear TA3FF inversion select prohibited. 11: Don't care 0: Disable 0: TMRA2 1: Enable...

Page 103 TMP91C824 TMRA register – TA0REG bit Symbol (0102H) Read/Write After reset Undefined – TA1REG bit Symbol (0103H) Read/Write After reset Undefined – TA2REG bit Symbol (010AH) Read/Write After reset Undefined – TA3REG bit Symbol (010BH) Read/Write After reset Undefined Note: The above registers are prohibited read-modify-write instruction. Figure 3.7.9 TMRA Registers 91C824-101 2008-02-20...

Page 104 TMP91C824 3.7.4 Operation in Each Mode (1) 8-bit timer mode Both TMRA0 and TMRA1 can be used independently as 8-bit interval timers. Setting its function or counter data for TMRA0 and TMRA1 after stop these registers. Generating interrupts at a fixed interval (using TMRA1) To generate interrupts at constant intervals using TMRA1 (INTTA1), first stop TMRA1

then set the operation mode, input clock and a cycle to TA01MOD and TA1REG register, respectively.

Page 105 TMP91C824 Generating a 50% duty ratio square wave pulse The state of the timer flip-flop (TA1FF) is inverted at constant intervals and its status output via the timer output pin (TA1OUT). Example: To output a 1.5 µs square wave pulse from the TA1OUT pin at fc = 33 MHz, use the following procedure to make the appropriate register settings.

Page 106 TMP91C824 Making TMRA1 count up on the match signal from the TMRA0 comparator Select 8-bit timer mode and set the comparator output from TMRA0 to be the input clock to TMRA1. Comparaot output (TMRA0 match) TMRA0 up counter (when TA0REG = 5) TMRA1 up counter (when TA1REG = 2) TMRA1 match output...

Page 107 TMP91C824 (2) 16-bit timer mode A 16-bit interval timer is configured by pairing the two 8-bit timers TMRA0 and TMRA1. To make a 16-bit interval timer in which TMRA0 and TMRA1 are cascaded together, set TA01MOD<TA01M1:0> to 01. In 16-bit timer mode, the overflow output from TMRA0 is used as the input clock for TMRA1, regardless of the value set in TA01MOD<TA01CLK1:0>.

Page 108 TMP91C824 (3) 8-bit PPG (Programmable pulse generation) output mode Square wave pulses can be generated at any frequency and duty ratio by TMRA0. The output pulses may be active-Low or active-High. In this mode TMRA1 cannot be used. TMRA0 outputs pulses on the TA1OUT pin. When <TA1FFC1:0>=”10”...

Page 109 TMP91C824 In this mode, a programmable square wave is generated by inverting the timer output each time the 8-bit up counter (UC0) matches the value in one of the timer registers TA0REG or TA1REG. The value set in TA0REG must be smaller than the value set in TA1REG. Although the up counter for TMRA1 (UC1) is not used in this mode, TA01RUN<TA1RUN>...

Page 110 TMP91C824 Example: To generate 1/4-duty 50-kHz pulses (at fc = 33 MHz) 20 µs * Clock state System clock: High frequency (fc) Clock gear: 1 (fc) Prescaler clock: f Calculate the value which should be set in the timer register. To obtain a frequency of 50 kHz, the pulse cycle t should be: t = 1/50 kHz = 20 µs φT1 = (2 /fc)s (at 33 MHz);...

Page 111 TMP91C824 (4) 8-bit PWM (Pulse width modulation) output mode This mode is only valid for TMRA0. In this mode, a PWM pulse with the maximum resolution of 8 bits can be output. When TMRA0 is used the PWM pulse is output on the TA1OUT pin. TMRA1 can also be used as an 8-bit timer.

Page 112 TMP91C824 In this mode, the value of the register buffer will be shifted into TA0REG if 2 overflow is detected when the TA0REG double buffer is enabled. Use of the double buffer facilitates the handling of low duty ratio waves. Match with TA0REG Up counter Up counter...

Page 113 TMP91C824 Table 3.7.3 PWM Cycle at fc = 33 MHz, fs = 32.768 kHz PWM Cycle Select Select Gear Value System Prescaler <GEAR2:0> Clock Clock φT1 φT4 φT16 φT1 φT4 φT16 φT1 φT4 φT16 <SYSCK> <PRCK1:0> 1 (fs) 15.6 ms 62.5 ms 250 ms 31.3 ms...

Page 114 TMP91C824 External Memory Extension Function (MMU) This is MMU function which can expand program/data area to 106 Mbytes by having 4 local areas. Address pins to external memory are 2 extended address bus pins (EA24, EA25) and 8 extended chip select pins ( ) in addition to 24 address bus pins (A0 to A23) which CS2A CS2E...

Page 115 TMP91C824 3.8.1 Recommendable Memory Map The recommendation logic address memory map at the time of varieties extension memory correspondence is shown in Figure 3.8.1. And, a physical-address map is shown in Figure 3.8.2. However, when memory area is less than 16 Mbytes and is not expanded, please refer to section of CS/WAIT controller.

Page 116 TMP91C824 LOCAL0 LOCAL1 LOCAL2 LOCAL3 for data ROM CS2A (16 Mbytes × 6) for data RAM for option for program ROM CS2B (8 Mbytes) program ROM (16 Mbytes) CS2E (16 Mbytes) 000000H BANK0 BANK0 BANK0 BANK1 BANK2 BANK12 BANK1 BANK0 BANK1 BANK3 BANK4...

Page 117 TMP91C824 3.8.2 Control Registers Setup bank value and bank use in bank setting register of each local area of LOCAL register in common area. Moreover, in that case, a combination pin is set up and mapping is simultaneously setup by the CS/WAIT controller. When CPU outputs logical address of the local area, MMU outputs physical address to the outside address bus pin according to value of bank setting register.

Page 118 TMP91C824 Data/Stack RAM SRAM 000000H to 1FFFFFH (Logical) 8 Mbytes 000000H to 7FFFFFH (Physical) 8 bits Optional ROM FLASH 400000H to 7FFFFFH (Logical) 16 Mbytes Data 000000H to FFFFFFH (Physical) 16 bits Address : SRAM) TMP91C824 Program ROM MROM 16 Mbytes C00000H to FFFFFFH (Logical) 16 bits 000000H to FFFFFFH (Physical)

Page 119 TMP91C824 At Figure 3.8.3, it shows example of connection TMP91C824 and some memories: Program ROM: MROM, 16 Mbytes, data ROM: MROM, 64 Mbytes, data RAM: SRAM, 8 Mbytes, 8-bit bus, option ROM: Flash, 16 Mbytes. In case of 16-bit bus memory connection, it need to shift 1-bit address bus from TMP91C824 and 8-bit bus case, direct connection address bus from TMP91C824.

Page 120 TMP91C824 ;BANK Operation ;***** ***** ORG 000000H ; Program ROM: Start address at BANK0 of LOCAL2 ORG 200000H ; Program ROM: Start address at BANK1 of LOCAL2 ORG 400000H ; Program ROM: Start address at BANK2 of LOCAL2 ORG 600000H ;...

Page 121 TMP91C824 ;BANK Operation ;***** ***** ORG 000000H ; Program ROM: Start address at BANK0 of LOCAL2 ORG 200000H ; Program ROM: Start address at BANK1 of LOCAL2 ; Operation at BANK1of LOCAL2 JP E00100H ; Jump to BANK7 (COMMON2) of LOCAL2 ORG 400000H ;...

Page 122 TMP91C824 At Figure 3.8.6, it shows example of program jump. In the same way with before example, two dot line squares show each ’s program ROM and ’s option ROM. Program start from E00000H common address, firstly, write to BANK register of LOCAL2 area upper 3-bit address of jumping point. After setting BANK1, jumping C00000H to DFFFFFH address: Logical LOCAL2 address, actually jump to physical 2000000H to 3FFFFFH address.

Page 123: Serial Channels

TMP91C824 Serial Channels TMP91C824 includes 2 serial I/O channels. For both channels either UART mode (Asynchronous transmission) or I/O interface mode (Synchronous transmission) can be selected. • I/O interface mode Mode 0: For transmitting and receiving I/O data using the synchronizing signal SCLK for extending I/O.

Page 124 TMP91C824 • Mode 0 (I/O interface mode) Bit0 Transfer direction • Mode 1 (7-bit UART mode) No parity Start Bit0 Stop Parity Start Bit0 Parity Stop • Mode 2 (8-bit UART mode) No parity Start Bit0 Stop Parity Stop Parity Start Bit0 •...

Page 125 TMP91C824 3.9.1 Block Diagrams Figure 3.9.2 is a block diagram representing serial channel 0. Prescaler φT0 16 32 64 φT2 φT8 φT32 Serial clock generation circuit BR0CR TA0TRG <BR0CK1:0> (from TMRA0) BR0CR BR0ADD <BR0S3:0> <BR0K3:0> φT0 UART mode φT2 SIOCLK φT8 φT32 BR0CR...

Page 126 TMP91C824 Prescaler φT0 16 32 64 φT2 φT8 φT32 Serial clock generation circuit BR1CR TA0TRG <BR1CK1:0> (from TMRA0) BR1CR BR1ADD <BR1S3:0> <BR1K3:0> φT0 UART SIOCLK mode φT2 φT8 φT32 BR1CR <BR1ADDE> SC1MOD0 SC1MOD0 Baud rate <SC1:0> <SM1:0> generator ÷2 SCLK1 interface mode Concurrent with PC5...

Page 127 TMP91C824 3.9.2 Operation of Each Circuit (1) Prescaler There is a 6-bit prescaler for generating a clock to SIO0. The clock selected using SYSCR<PRCK1:0> is divided by 4 and input to the prescaler as φT0. The prescaler can be run by selecting the baud rate generator as the serial transfer clock. Table 3.9.2 shows prescaler clock resolution into the baud rate generator.

Page 128 TMP91C824 (2) Baud rate generator The baud rate generator is the circuit which generates transmission and receiving clocks which determine the transfer rate of the serial channels. The input clock to the baud rate generator, φT0, φT2, φT8 or φT32, is generated by the 6-bit prescaler which is shared by the timers.

Page 129 TMP91C824 • Integer divider (N divider) For example, when the source clock

frequency (fc) = 12.288 MHz, the input clock frequency = φT2 (fc/16), the frequency divider N (BR0CR<BR0S3:0>) = 5, and BR0CR<BR0ADDE> = 0, the baud rate in UART mode is as follows: * Clock state System clock: High frequency (fc)

Page 130 TMP91C824 Table 3.9.3 Transfer Rate Selection (when baud rate generator Is used and BR0CR<BR0ADDE> = 0) Unit (kbps) Input Clock φT0 φT2 φT8 φT32 Frequency Divider fc [MHz] (set to BR1CR<BR1S3:0>) 9.830400 76.800 19.200 4.800 1.200 ↑ 38.400 9.600 2.400 0.600 ↑...

Page 131 TMP91C824 (3) Serial clock generation circuit This circuit generates the basic clock for transmitting and receiving data. • In I/O interface mode In SCLK output mode with the setting SC0CR<IOC> = 0, the basic clock is generated by dividing the output of the baud rate generator by 2, as described previously.

Page 132 TMP91C824 (6) The receiving buffers To prevent overrun errors, the receiving buffers are arranged in a double-buffer structure. Received data is stored one bit at a time in receiving buffer 1 (which is a shift register). When 7 or 8 bits of data have been stored in receiving buffer 1, the stored data is transferred to receiving buffer 2 (SC0BUF);...

Page 133 TMP91C824 Handshake function Use of pin allows data can be sent in units of one frame; thus, overrun errors can be avoided. The handshake functions is enabled or disabled by the SC0MOD<CTSE> setting. When the pin goes high on completion of the current data send, data transmission is halted until the pin goes low again.

Page 134 TMP91C824 (9) Transmission buffer The transmission buffer (SC0BUF) shifts out and sends the transmission data written from the CPU form the least significant bit (LSB) in order. When all the bits are shifted out, the transmission buffer becomes empty and generates an INTTX0 interrupt.

Page 135 TMP91C824 (12) Timing generation In UART mode Receiving 8 Bits + Parity 8 Bits, 7 Bits + Parity, Mode 9 Bits (Note) (Note) 7 Bits Interrupt timing Center of last bit Center of last bit Center of stop bit (Bit8) (Parity bit) Framing error timing Center of stop bit...

Page 136 TMP91C824 3.9.3 SFRs Bit symbol CTSE SC0MOD0 (0202H) Read/Write After reset Function Transfer Handshake Receive Wakeup Serial transmission Serial transmission clock data bit8 function function mode (UART) 0: CTS 00: I/O interface mode 00: TMRA0 trigger disable 0: Receive 0: Disable 01: 7-bit UART mode 01: Baud rate 1: CTS...

Page 137 TMP91C824 SC1MOD0 Bit symbol CTSE (020AH) Read/Write After reset Function Transfer Handshake Receive Wakeup Serial transmission Serial transmission data bit8 0: CTS function function mode clock (UART) disable 0: Receive 0: Disable 00: I/O interface mode 00: TMRA0 trigger 1: CTS disable 1: Enable 01: 7-bit UART mode...

Page 138 TMP91C824 SC0CR Bit symbol EVEN OERR PERR FERR SCLKS (0201H) Read/Write R (Cleared to 0 when read) After reset Undefined Function Received Parity Parity 1: Error 0: SCLK0 0: Baud data bit8 0: Odd addition rate 1: Even 0: Disable generator 1: Enable 1: SCLK0...

Page 139 TMP91C824 SC1CR Bit symbol EVEN OERR PERR FERR SCLKS (0209H) Read/Write R (Cleared to 0 when) After reset Undefined Function Received Parity Parity 1: Error 0: SCLK1 0: Baud rate data bit8 0: Odd addition generator 1: Even 0: Disable 1: SCLK1 1: Enable 1: SCLK1...

Page 140 TMP91C824 − BR0CR Bit symbol BR0ADDE BR0CK1 BR0CK0 BR0S3 BR0S2 BR0S1 BR0S0 (0203H) Read/Write After reset 00: φT0 + (16 − K)/16 Function Always Setting the divided frequency “N” 01: φT2 write 0 division (0 to F) 10: φT8 0: Disable 11: φT32 1: Enable + (16 −...

Page 141 TMP91C824 − BR1CR Bit symbol BR1ADDE BR1CK1 BR1CK0 BR1S3 BR1S2 BR1S1 BR1S0 (020BH) Read/Write After reset 00: φT0 + (16 − K)/16 Function Always Setting the divided frequency “N” 01: φT2 write 0 division (0 to F) 10: φT8 0: Disable 11: φT32 1: Enable + (16 −...

Page 142 TMP91C824 (Transmission) SC0BUF (0200H) (Receiving) Note: Prohibit read modify write for SC0BUF. Figure 3.9.13 Serial Transmission/Receiving Buffer Registers (SIO0, SC0BUF) Bit symbol I2S0 FDPX0 SC0MOD1 (0205H) Read/Write After reset Function IDLE2 Duplex 0: Stop

0: Half 1: Run 1: Full Figure 3.9.14 Serial Mode Control Register 1 (SIO0, SC0MOD1) 91C824-140 2008-02-20...

Page 143 TMP91C824 (Transmission) SC1BUF (0208H) (Receiving) Note: Prohibit read modify write for SC1BUF. Figure 3.9.15 Serial Transmission/Receiving Buffer Registers (SIO1, SC1BUF) SC1MOD1 Bit symbol I2S1 FDPX1 (020DH) Read/Write After reset Function IDLE2 Duplex 0: Stop 0: Half 1: Run 1: Full Figure 3.9.16 Serial Mode Control Register 1 (SIO1, SC1MOD1) 91C824-141 2008-02-20...

Page 144: Operation In Each Mode

TMP91C824 3.9.4 Operation in Each Mode (1) Mode 0 (I/O interface mode) This mode allows an increase in the number of I/O pins available for transmitting data to or receiving data from an external shift register. This mode includes the SCLK output mode to output synchronous clock SCLK and SCLK input mode to input external synchronous clock SCLK.

Page 145 TMP91C824 Transmission In SCLK output mode 8-bit data and a synchronous clock are output on the TXD0 and SCLK0 pins respectively each time the CPU writes the data to the transmission buffer. When all data is output, INTES0<ITX0C> will be set to generate the INTTX0 interrupt.

Page 146 TMP91C824 Receiving In SCLK output mode, the synchronous clock is outputted from SCLK0 pin and the data is shifted to receiving buffer 1. This starts when the receive interrupt flag INTES0<IRX0C> is cleared by reading the received data. When 8- bit data are received, the data will be transferred to receiving buffer 2 (SC0BUF according to the timing shown below) and INTES0<IRX0C>...

Page 147 TMP91C824 Transmission and receiving (Full duplex mode) When the full duplex mode is used, set the level of Receive Interrupt to 0 and set enable the interrupt level (1 to 6) to the transfer interrupt. In the transfer interrupt program, The receiving operation should be done like the above example before setting the next transfer data.

Page 148 TMP91C824 (2) Mode 1 (7-bit UART mode) 7-bit UART mode is selected by setting serial channel mode register SC0MOD0<SM1:0> to 01. In this mode, a parity bit can be added. Use of a parity bit is enabled or disabled by the setting of the serial channel control register SC0CR<PE>...

Page 149 TMP91C824 * Clock state System clock: High frequency (fc) Clock gear: 1 (fc) Prescaler clock: System clock Main settings 7 6 5 4 3 2 1 0 ← X X − − − − 0 − PCCR Set PC1 to function as the RXD0 pin. SC0MOD0 ←...

Page 150 TMP91C824 Protocol (1) Select 9-bit UART mode on the master and slave controllers. (2) Set the SC0MOD0<WU> bit on each slave controller to 1 to enable data receiving. (3) The master controller transmits one-frame data including the 8-bit select code for the slave controllers.

Page 151 TMP91C824 Example: To link two slave controllers serially with the master controller using the internal clock f as the transfer clock. Master Slave 1 Slave 2 Select code Select code 00000001 00001010 Since serial channels 0 and 1 operate in exactly the same way, channel 0 only is used for the purposes of this explanation.

Page 152 TMP91C824 3.9.5 Support for IrDA SIO0 includes support for the IrDA 1.0 infrared data communication specification. Figure 3.9.24 shows the block diagram. Transmisison data TXD0 IR modulator IR transmitter & LED IR output SIO0 Modem Receive data RXD0 IR demodulator IR receiver IR input TMP91C824...

Page 153: Data Format

TMP91C824 (3) Data format The data format is fixed as follows: • Data length: 8-bit • Parity bits: none • Stop bits: 1 Any other settings don’t guarantee the normal operation. (4) SFR Figure 3.9.27 shows the control register SIRCR. Set the data SIRCR during SIO0 is inhibited (Both TXEN and RXEN of this register should be set to 0).

Page 154 TMP91C824 As the same reason, + (16 − k)/16 division functions in the baud rate generator of SIO0 can not be used to generate 115.2 kbps baud rate. Also when the 38.4 kbps

and 1/16 pulse width, + (16 − k)/16 division function can not be used.

Page 155 TMP91C824 Bit symbol PLSEL RXSEL TXEN RXEN SIRWD3 SIRWD2 SIRWD1 SIRWD0 SIRCR (0207H) Read/Write After reset Function Select Receive Transmit Receive Select receive pulse width transmit data 0: Disable 0: Disable Set effective pulse width for equal or more than 2x ×...

Page 156 TMP91C824 3.10 Serial Bus Interface (SBI) The TMP91C824FG has a 1-channel serial bus interface which employs a clocked- synchronous 8-bit SIO mode and an I C bus mode. The serial bus interface is connected to an external device through P71 (SDA) and P72 (SCL) in the I C bus mode;...

Page 157 TMP91C824 3.10.2 Serial Bus Interface (SBI) Control The following registers are used to control the serial bus interface and monitor the operation status. • Serial bus interface control register 1 (SBI0CR1) • Serial bus interface control register 2 (SBI0CR2) • Serial bus interface data buffer register (SBI0DBR) •...

Page 158 TMP91C824 3.10.4 C Bus Mode Control The following registers are used to control and monitor the operation status when using the serial bus interface (SBI) in the I C bus mode. Seirial Bus Interface Conrol Register 1 SCK0/ SBI0CR1 Bit symbol SCK2 SCK1 SWRMON...

Page 159 TMP91C824 Serial Bus Interface Control Register 2 SBI0CR2 Bit symbol SBIM1 SBIM0 SWRST1 SWRST0 (0243H) Read/Write W (Note 1) W (Note 1) After reset Prohibit Function Master/slave Transmitter/ Start/stop Cancel Serial bus interface Software reset generate read- selection receiver condition INTSBI operating mode selection write 10 and 01, then an...

Page 160 TMP91C824 Serial Bus Interface Status Register SBI0SR Bit symbol (0243H) Read/Write After reset Prohibit Function Master/ Transmitter/ C bus INTSBI Arbitration Slave GENERAL Last read- slave receiver status interrupt lost address CALL received bit modify- write status status monitor request detection match detection...

Page 161 TMP91C824 Serial Bus Interface Baud Rate Regster 0 − SBI0BR0 Bit symbol I2SBI0 (0244H) Read/Write Prohibit After reset read- Function Always IDLE2 modify- write write 0 0: Stop 1: Run Operation during IDLE 2 mode Stop Operation Serial Bus Interface Baud Rate Register 1 −...

Page 162 TMP91C824 3.10.5 Control in I C Bus Mode (1) Acknowledge mode specification Set the SBI0CR1<ACK> to 1 for operation in the acknowledge mode. The TMP91C824 generates an additional clock pulse for an acknowledge signal when operating in master mode. In the transmitter mode during the clock pulse cycle, the SDA pin is released in order to receive the acknowledge signal from the receiver.

Page 163 TMP91C824 Clock synchronization In the I C bus mode, in order to wired-AND a bus, a master device which pulls down a clock line to low level, in the first place, invalidate a clock pulse of another master device which generates a high-level clock pulse. The master device with a high-level clock pulse needs to detect the situation and implement the following procedure.

Page 164 TMP91C824 (6) Transmitter/receiver selection Set the SBI0CR2<TRX> to 1 for operating the TMP91C824 as a transmitter. Clear the <TRX> to 0 for operation as a receiver. When data with an addressing format is transferred in slave mode, when a slave address with the same value that an I2C0AR or a GENERAL CALL is received (All 8-bit data are 0 after a start condition), the <TRX>...

Page 165 TMP91C824 (8) Interrupt service requests and interrupt cancellation When a serial bus interface interrupt request (INTSBI) occurs, the SBI0CR2<PIN> is cleared to 0. During the time that the SBI0CR2<PIN> is 0, the SCL line is pulled down to the low level. The <PIN>...

Page 166 TMP91C824 The TMP91C824 compares the levels on the bus’s SDA line with those of the internal SDA output on the rising edge of the SCL line. If the levels do not match, arbitration is lost and SBI0SR<AL> is set to 1. When SBI0SR<AL>...

Page 167 TMP91C824 (14) Software reset function The software reset function is used to initialize the SBI circuit, when SBI is locked by external noises, etc. An internal reset signal pulse

can be generated by setting SBI0CR2<SWRST1:0> to 10 and 01. This initializes the SBI circuit internally. All command (except SBI0CR2<SBIM1:0>) registers and status registers are initialized as well.

Page 168 TMP91C824 3.10.6 Data Transfer in I C Bus Mode (1) Device initialization Set the SBI0BR1<P4EN>, SBI0CR1<ACK, SCK2:0>, Set SBI0BR1 to 1 and clear bits 7 to 5 and 3 in the SBI0CR1 to 0. Set a slave address <SA6:0> and the <ALS> (<ALS> = 0 when an addressing format) to the I2C0AR.

Page 169 TMP91C824 (3) 1-word data transfer Check the <MST> by the INTSBI interrupt process after the 1-word data transfer is completed, and determine whether the mode is a master or slave. If <MST> = 1 (Master mode) Check the <TRX> and determine whether the mode is a transmitter or receiver. When the <TRX>...

Page 170 TMP91C824 When the <TRX> is 0 (Receiver mode) When the next transmitted data is other than 8 bits, set <BC2:0> <ACK> and read the received data from SBI0DBR to release the SCL line (data which is read immediately after a slave address is sent is undefined). After the data is read, <PIN>...

Page 171 TMP91C824 If <MST> = 0 (Slave mode) In the slave mode the TMP91C824 operates either in normal slave mode or in slave mode after losing arbitration. In the slave mode, an INTSBI interrupt request occurs when the TMP91C824 receives a slave address or a GENERAL CALL from the master device, or when a GENERAL CALL is received and data transfer is complete, or after matching received address.

Page 172 TMP91C824 (4) Stop condition generation When SBI0SR<BB> = 1, the sequence for generating a stop condition can be initiated by writing 1 to SBI0CR2<MST, TRX, PIN> and 0 to SBI0CR2<BB>. Do not modify the contents of SBI0CR2<MST, TRX, PIN, BB> until a stop condition has been generated on the bus.

Page 173 TMP91C824 (5) Restart Restart is used during data transfer between a master device and a slave device to change the data transfer direction. The following description explains how to restart when the TMP91C824 is in master mode. Clear SBI0CR2<MST, TRX, BB> to 0 and set SBI0CR2<PIN> to 1 to release the bus.

Page 174 TMP91C824 3.10.7 Clocked Synchronous 8-Bit SIO Mode Control The following registers are used to control and monitor the operation status when the serial bus interface (SBI) is being operated in clocked synchronous 8-bit SIO mode. Serial Bus Interface Control Register 1 SBI0CR1 Bit symbol SIOS...

Page 175 TMP91C824 Serial Bus Interface Control Register 2 − − SBI0CR2 Bit symbol SBIM1 SBIM0 (0243H) Read/Write After reset Prohibit Function Serial bus interface (Note 2) (Note 2) read- operation mode modify- selection write 00: Port mode 01: SIO mode 10: I C bus mode 11: (Reserved) Serial bus interface operation mode selection...

Page 176 TMP91C824 Serial Bus Interface Baud Rate Register 0 − SBI0BR0 Bit symbol I2SBI0 (0244H) Read/Write After reset Prohibit read- Function Always IDLE2 modify- write 0 0: Stop write 1: Operate Operation in IDLE2 mode Stop Operate Serial Bus Interface Baud Rate Register 1 −...

Page 177: Serial Clock

TMP91C824 (1) Serial clock Clock source SBI0CR1<SCK2:0> is used to select the following functions: Internal clock In internal clock mode one of seven frequencies can be selected. The serial clock signal is output to the outside on the SCK pin. The SCK pin goes high when data transfer starts.

Page 178 TMP91C824 Shift edge Data is transmitted on the leading edge of the clock and received on the trailing edge. Leading edge shift Data is shifted on the leading edge of the serial clock (on the falling edge of the SCK pin input/output). Trailing edge shift Data is shifted on the trailing edge of the serial clock (on the rising edge of the SCK pin input/output).

Page 179 TMP91C824 (2) Transfer modes The SBI0CR1<SIOM1:0> is used to select a transmit, receive or transmit/receive mode. 8-bit transmit mode Set a control register to a transmit mode and write transmit data to the SBI0DBR. After the transmit data is written, set

the SBI0CR1<SIOS> to 1 to start data transfer.

Page 180 TMP91C824 Example: Program to stop data transmission (when an external clock is used) Clear <SIOS> <SIOS> <SIOF> <SEF> SCK pin (Output) SO pin INTSBI interrupt request SBI0DBR (a) Internal clock Write transmitted data Clear <SIOS> <SIOS> <SIOF> <SEF> SCK pin (Input) SO pin INTSBI interrupt request...

Page 181 TMP91C824 8-bit receive mode SCK pin SIOF SO pin Bit6 Bit7 = 3.5/f SODH Figure 3.10.27 Transmitted Data Hold Time at End of Transmission Set the control register to receive mode and set SBI0CR1<SIOS> to 1 for switching to receive mode. Data is received into the shift register via the SI pin and synchronized with the serial clock, starting from the least significant bit (LSB).

Page 182 TMP91C824 Clear <SIOS> <SIOS> <SIOF> <SEF> SCK pin (Output) SI pin INTSBI interrupt request SBI0DBR Read receiver data Read receiver data Figure 3.10.28 Receiver Mode (Example: Internal clock) 8-bit transmit/receive mode Set a control register to a transmit/receive mode and write data to SBI0DBR. After the data has been written, set SBI0CR<SIOS>...

Page 183 TMP91C824 Clear <SIOS> <SIOS> <SIOF> <SEF> SCK pin (Output) SO pin SI pin INTSBI interrupt request SBI0DBR Write transmitted Read received Write transmitted Read received data (a) data (c) data (b) data (d) Figure 3.10.29 Transmit/Received Mode (Example using internal clock) SCK pin SIOF SO pin...

Page 184 TMP91C824 3.11 Analog/Digital Converter The TMP91C824 incorporates a 10-bit successive approximation-type analog/digital converter (AD converter) with 8-channel analog input. Figure 3.11.1 is a block diagram of the AD converter. The 8-channel analog input pins (AN0 to AN7) are shared with the input only port 8 and can thus be used as an input port. Note: When IDLE2, IDLE1 or STOP mode is selected, so as to reduce the power, with some timings the system may enter a standby mode even though the internal comparator is still enabled.

Page 185 TMP91C824 3.11.1 Analog/Digital Converter Registers The AD converter is controlled by the two AD mode control registers: ADMOD0 and ADMOD1. The AD conversion results are stored in 8 kinds of AD conversion data upper and lower registers: ADREG04H/L, ADREG15H/L, ADREG26H/L and ADREG37H/L. Figure 3.11.2 shows the registers related to the AD converter.

Page 186 TMP91C824 AD Mode Control Register 1 ADMOD1 Bit symbol VREFON I2AD ADTRGE ADCH2 ADCH1 ADCH0 (02B1H) Read/Write After reset Function VREF IDLE2 Analog input channel selection AD external application 0: Stop trigger start control 1: Operate control 0: OFF 0: Disable 1: ON 1: Enable Analog input channel selection...

Page 187 TMP91C824 AD Conversion Data Low Register 0/4 ADREG04L Bit symbol ADR01 ADR00 ADR0RF (02A0H) Read/Write After reset Undefined Function Stores lower 2 bits of AD conversion result conversion data storage flag 1: Conversion result stored AD Conversion Data Upper Register 0/4 ADREG04H Bit symbol ADR09...

Page 188 TMP91C824 AD Conversion Result Lower Register 2/6 ADREG26L Bit symbol ADR21 ADR20 ADR2RF (02A4H) Read/Write After reset Undefined Function Stores lower 2 bits of AD conversion AD conversion result. data storage flag 1: Conversion result stored AD Conversion Data upper Register 2/6 ADREG26H Bit symbol ADR29...

Page 189 TMP91C824 3.11.2 Description of Operation (1) Analog reference voltage A high-level analog reference voltage is applied to the VREFH pin; a low-level analog reference voltage is applied to the VREFL pin. To perform AD conversion, the reference voltage as the difference between VREFH and VREFL, is divided by 1024 using string resistance.

Page 190 TMP91C824 (3) Starting AD conversion To start AD conversion, write 1 to ADMOD0<ADS> in AD mode control register 0 or ADMOD1<ADTRGE> in AD mode control register 1 and input falling edge on pin. When conversion starts, conversion busy flag ADTRG ADMOD0<ADBF>...

Page 191 TMP91C824 Channel fixed repeat conversion mode Setting ADMOD0<REPEAT> and ADMOD0<SCAN> to 10 selects channel fixed repeat conversion mode. In this mode, data on one specified channel is converted repeatedly. When conversion been completed, ADMOD0<EOCF> ADMOD0<ADBF> is not cleared to 0 but held 1. INTAD interrupt request

generation timing is determined by the setting of ADMOD0<ITM0>.

Page 192 TMP91C824 (5) AD conversion time 84 states (5.1 µs at f = 33 MHz) are required for the AD conversion for one channel. (6) Storing and reading the results of AD conversion conversion data upper lower registers (ADREG04H/L ADREG37H/L) store the AD conversion results. (ADREG04H/L to ADREG37H/L are read-only registers.) In channel fixed repeat conversion mode, the conversion results are stored successively in registers ADREG04H/L to ADREG37H/L.

Page 193 TMP91C824 Example: Convert the analog input voltage on the AN3 pin and write the result, to memory address 0800H using the AD interrupt (INTAD) processing routine. Main routine: 7 6 5 4 3 2 1 0 ← – 1 0 0 – – – – INTE0AD Enable INTAD and set it to interrupt level 4.

Page 194 TMP91C824 3.12 Watchdog Timer (Runaway detection timer) The TMP91C824 features a watchdog timer for detecting runaway. The watchdog timer (WDT) is used to return the CPU to normal state when it detects that the CPU has started to malfunction (Runaway) due to causes such as noise. When the watchdog timer detects a malfunction, it generates a non-maskable interrupt INTWD to notify the CPU.

Page 195 TMP91C824 The watchdog timer consists of a 22-stage binary counter which uses the system clock) as the input clock. The binary counter can output f WDT counter Overflow WDT interrupt Write clear code WDT clear (Software) Figure 3.12.2 NORMAL Mode The runaway is detected when an overflow occurs, and the watchdog timer can reset device.

Page 196 TMP91C824 3.12.2 Control Registers The watchdog timer WDT is controlled by two control registers WDMOD and WDCR. (1) Watchdog timer mode register (WDMOD) Setting the detection time for the watchdog timer in <WDTP1:0> This 2-bit register is used for setting the watchdog timer interrupt time used when detecting runaway.

Page 197 TMP91C824 WDMOD − Bit symbol WDTE WDTP1 WDTP0 I2WDT RESCR (0300H) Read/Write After reset Function Select detecting time IDLE2 1: Internally Always control 00: 2 0: Stop connects write 0 1: Enable 1: Operate WDL out to 01: 2 the reset 10: 2 11: 2 Watchdog timer out control...

Page 198 TMP91C824 − Bit symbol WDCR Read/Write (0301H) − After reset Prohibit Function B1H: WDT disable code read- modify- 4EH: WDT clear code write Disable/clear WDT Disable code Clear code Others Don’t care Figure 3.12.5 Watchdog Timer Control Register 91C824-196 2008-02-20...

Page 199 TMP91C824 3.12.3 Operation The watchdog timer generates an INTWD interrupt when the detection time set in the WDMOD<WDTP1:0> has elapsed. The watchdog timer must be cleared 0 by software before an INTWD interrupt will be generated. If the CPU malfunctions (e.g., if runaway occurs) due to causes such as noise, but does not execute the instruction used to clear the binary counter, the binary counter will overflow and an INTWD interrupt will be generated.

Page 200: Real Time Clock (Rtc)

TMP91C824 3.13 Real Time Clock (RTC) 3.13.1 Function Description for RTC (1) Clock function (Second, minute, Hour, day of the week, day, Month and leap year) (2) Calendar function (3) 24- or 12-hour (AM/PM) clock function (4) ± 30 second adjustment function (by software) (5) Alarm output 1Hz/16Hz (from pin) ALARM...

Page 201 TMP91C824 3.13.3 Control Registers Table 3.13.1 PAGE 0 (Clock function) Registers Symbol Address Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 Function Read/Write SECR 0320H 40 s 20 s 10 s Second column MINR 0321H 40 min. 20 min. 10 min. 8 min.

Page 202 TMP91C824 3.13.4 Detailed Explanation of Control Register RTC is not initialized by reset. Therefore, all registers must be initialized at the beginning of the program. (1) Second column register (for PAGE0 only) SECR Bit symbol (0320H) Read/Write After reset Undefined Function "0"...

Page 203 TMP91C824 (2) Minute column register (for PAGE0/1) MINR Bit symbol (0321H) Read/Write After reset Undefined Function "0" is read. 40 min, 20 min, 10 min, 8 min, 4 min, 2

min, 1 min, column column column column column column column 0 min.

Page 204 TMP91C824 (3) Hour column register (for PAGE0/1) In case of 24-hour clock mode (MONTHR<MO0>=1) of PAGE1 HOURR Bit symbol (0322H) Read/Write After reset Undefined Function "0" is read. 20 hour 10 hour 8 hour 4 hour 2 hour 1 hour column column column...

Page 205 TMP91C824 (4) Day of the week column register (for PAGE0/1) DAYR Bit symbol (0323H) Read/Write After reset Undefined Function "0" is read. Sunday Monday Tuesday Wednesday Thursday Friday Saturday Note: Do not set the data other than showing above. (5) Day column register (for PAGE0/1) DATER Bit symbol (0324H)

Page 206 TMP91C824 (6) Month column register (for PAGE0 only) MONTHR Bit symbol (0325H) Read/Write After reset Undefined Function "0" is read. 10 months 8 months 4 months 2 months 1 month January February March April June July August September October November December Note: Do not set the data other than showing above.

Page 207 TMP91C824 (8) Year column register (for PAGE0 only) YEARR Bit symbol (0326H) Read/Write After reset Undefined Function 80 Years 40 Years 20 Years 10 Years 8 Years 4 Years 2 Years 1 Year 00 years 01 years 02 years 03 years 04 years 05 years 99 years...

Page 208 TMP91C824 (10) PAGE register setting (for PAGE0/1) PAGER Bit symbol INTENA ADJUST ENATMR ENAALM PAGE (0327H) Read/Write Read-modify After reset Undefined Undefined Undefined write Function “0” is read. INTRTC 0:Don’t care Clock ALARM PAGE instruction 0: Disable 1:Adjust 0: Disable 0: Disable selection “0”...

Page 209 TMP91C824 3.13.5 Operational Description (1) Reading Clock data There is the case which reads wrong data when carry of the inside counter happens during the operation which Clock data reads. Therefore, please read two times with the following way for reading correct data. Start PAGER<PAGE>...

Page 210 TMP91C824 (2) Timing of INTRTC and Clock data When time is read by interrupt, read clock data within 0.5s(s) after generating interrupt. This is because count up of clock data occurs by rising edge of 1Hz pulse cycle. ALARM INTRTC 1s counter (Internal signal) 1s count UP...

Page 211 TMP91C824 (3) Writing Clock data When there is carry on the way of write operation, expecting data can not be wrote exactly. Therefore, in order to write in data exactly please follow the below way. Reset for a divider Inside of RTC, there is 15-stage divider which generates 1 Hz clock from 32.768 kHz.

Page 212 TMP91C824 Disabling the Clock Carry of a clock is prohibited when write “0” to PAGER<ENATMR> and can prevent malfunction by 1s carry hold circuit. During a clock prohibited, 1s carry hold circuit holds one second carry signal, which is generated from divider. After becoming clock enable state, output the carry signal to clock and revise time and continue operation.

Page 213 TMP91C824 3.13.6 Explanation of the Alarm Function Can use alarm function by setting of register of PAGE1 and output either of three signals from pin as follows by write “1” to PAGER<PAGE>. INTRTC outputs ALARM 1shot pulse when the falling edge is detected. RTC is not initializes by RESET. Therefore, when clock or alarm function is used, clear interrupt request flag in INTC (interrupt controller).

Page 214 TMP91C824 (4) When output clock of 1 Hz pin by setting up PAGER<ENAALM> = 0, RTC outputs clock of 1 Hz to ALARM RESTR<DIS1HZ> = 0, <DIS16HZ> = 1. And RTC generates INTRTC interrupt by falling edge of the clock. (5) When output clock of 16 Hz RTC outputs clock of 16 Hz to pin by setting up PAGER<ENAALM>...

Page 215 TMP91C824 3.14 Melody/Alarm Generator (MLD) TMP91C824 incorporates melody function and alarm function, both of which are output from the MLDALM pin. 5 kinds of fixed cycle interrupts are generated by the 15-bit free-run counter, which is used for alarm generator. Features are as follows.

Page 216 TMP91C824 3.14.1 Block Diagram Internal data bus [Melody generator] Reset MELFH, MELFL register MELFH <MELON> MELOUT Invert Comparator (CP0) Stop&clear Clear

Low-speed 12-bit counter (UC0) clock (32.76 kHz) INTALM0 (8192 Hz) INTALM1 (512 Hz) Edge INTALM2 (64 Hz) detector INTALM3 (2 Hz) INTALM4 (1 Hz) 15-bit counter (UC1) INTALMH...

Page 217 TMP91C824 3.14.2 Control Registers ALM Register Bit symbol (0330H) Read/Write After reset Function Setting alarm pattern MELALMC Register − − − − MELALMC Bit symbol ALMINV MELALM (0331H) Read/Write After reset Function Free-run counter control Alarm Always write 0 Output 00: Hold waveform waveform...

Page 218 TMP91C824 3.14.3 Operational Description (1) Melody generator The melody function generates signals of any frequency (4 Hz to 5461 Hz) based on low-speed clock (32.768 kHz) and outputs the signals from the MLDALM pin. By connecting a loud speaker outside, melody tone can sound easily. (Operation) At first, MELALMC<MELALM>...

Page 219 TMP91C824 (2) Alarm generator The alarm function generates 8 kinds of alarm waveform having a modulation frequency 4096 Hz determined by the low-speed clock (32.768 kHz). And this waveform is reversible by setting a value to a register. By connecting a loud speaker outside, alarm tone can sound easily. 5 kinds of fixed cycle (1 Hz, 2 Hz, 64 Hz, 512 Hz and 8192 Hz) interrupts are generated by the free-run counter, which is used for alarm generator.

Page 220 TMP91C824 Example: Waveform of alarm pattern for each setting value: Not invert AL1 pattern Modulation frequency (4096 Hz) (Continuous output) AL2 pattern (8 times/1 s) 31.25 ms AL3 pattern 500 ms (once) AL4 pattern (Twice/1 s) 62.5 ms AL5 pattern (3 times/1 s) 62.5 ms AL6 pattern...

Page 221: Electrical Characteristics

TMP91C824 Electrical Characteristics Absolute Maximum Ratings Parameter Symbol Rating Unit −0.5 to 4.0 Power supply voltage −0.5 to Vcc + 0.5 Input voltage Output current −2 Output current ΣIOL Output current (total) ΣIOH −80 Output current (total) Power dissipation (Ta = 85°C) Soldering temperature (10 s) TSOLDER −65 to 150...

Page 222 TMP91C824 DC Characteristics (1/2) Typ. Parameter Symbol Condition Unit (Note) Power supply voltage fc = 2 to 33 MHz fs = 30 to (AVCC = DVCC) 34 kHz fc = 2 to 10 MHz (AVSS = DVSS = 0 V) Vcc ≥...

Page 223 TMP91C824 DC Characteristics (2/2) Typ. Parameter Symbol Condition Unit (Note1) 0.0 ≤ VIN ≤ Vcc ±5 Input leakage current 0.02 μA 0.2 ≤ VIN ≤ Vcc − 0.2 ±10 Output leakage current 0.05 VIL2 = 0.2 Vcc, Power down voltage VSTOP VIH2 = 0.8 Vcc (at STOP, RAM back up)

Page 224 TMP91C824 AC Characteristics (1) Vcc = 3.0 V ± 10% = 33 MHz Variable Parameter Symbol Unit period (= x) 30.3 31250 30.3 A0 to A23 valid → x − 23 fall rise → A0 to A23 hold 0.5x −13 rise →...

Page 225 TMP91C824 (2) Vcc = 2.0 V ± 10% Variable 10 MHz Parameter Symbol Unit period (= x) tFPH 31250 2 A0 to A15 valid → x − 46 fall rise → A0 to A23 hold 0.5x − 30 tCAR rise → A0 to A23 hold x −...

Page 226: Read Cycle

Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

Page 227: Write Cycle

Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

Page 228: Ad Conversion Characteristics

TMP91C824 AD Conversion Characteristics AVcc = Vcc, AVss = Vss Parameter Symbol Condition Typ. Unit 3.6 V ≥ V ≥ 2.7 V − 0.2 V Analog reference voltage (+) VREFH = 2 V ± 10% Vss + 0.2 V 3.6 V ≥ V ≥...

Page 229 TMP91C824 Serial Channel Timing (I/O Internal Mode) (1) SCLK input mode Variable 10 MHz 27 MHz Parameter Symbol Unit Min Max Min Max µs SCLK period 0.59 Output data Vcc = 3 V ± 10% /2 − 4X − 110 →...

Page 230 TMP91C824 Event Counter (TA0IN) Variable 10 MHz 27 MHz Parameter Symbol Unit 8X + 100 Clock period 4X + 40 Clock low level width VCKL 4X + 40 Clock high level width VCKH Interrupt, Capture , INT0 to INT3 interrupts Variable 10 MHz 27 MHz...

Page 231 TMP91C824 Bus Request/Bus Acknowledge BUSRQ BUSAK (Note 1) CBAL (Note 2) AD0 to AD15 A0 to A23, (Note 2) = 4 MHz = 16 MHz Variable Symbol Parameter Unit Output buffer off to BUSAK high to output buffer on BUSAK Note 1: Even if the signal goes low, the bus will not be released while the signal is low.

Page 232 TMP91C824 4.10 Recommended Crystal Oscillation Circuit TMP91C824 is evaluated by below oscillator vender. When selecting external parts, make use of this information. Note: Total loads value of oscillator is sum of external loads (C1 and C2) and floating loads of actual assemble board.

Page 233 TMP91C824 (2) TMP91C824 recommended ceramic oscillator: Murata Manufacturing Co., Ltd. (JAPAN) Circuit parameter recommended Parameter of Elements Running Condition Oscillation Item of Oscillator Frequency Voltage of Tc [°C] [MHz] [pF] [pF] [Ω] [Ω] Power [V] 2.00 CSTLS2M00G56-B0 (47) (47) Open 2.50 CSTLS2M50G56-B0 (47)

Page 234 TMP91C824 Table of SFRs The SFRs (Special function registers) include the I/O ports and peripheral control registers allocated to the 4-Kbyte address space from 000FE0H to 000FFFH. (1) I/O port (2) I/O port control (3) Interrupt control (4) Chip select/wait control (5) Clock gear (6) DFM (Clock doubler) (7) 8-bit timer...

Page 235 TMP91C824 Table 5.1 Address Map SFRs [1], [2] Port Address Name Address Name Address Name 0000H 0010H 0022H P1CR PBCR P6FC PBFC P7CR PCCR P7FC PCFC PCODE P2FC P5CR PDFC P5FC P6FC2 P7FC2 P7ODE [3] INTC Address Name Address Name Address Name 0070H...

Page 236 TMP91C824 Table 5.2 Address Map SFRs [7] TMRA Address Name 0100H TA01RUN TA0REG TA1REG TA01MOD TA01FFCR TA23RUN TA2REG TA3REG TA23MOD TA3FFCR [8] UART/SIO [9] I C bus/SIO Address Name Address Name 0200H SC0BUF 0240H SBI0CR1 SC0CR SBI0DBR SC0MOD0 I2C0AR BR0CR SBI0CR2/SBI0SR BR0ADD SBI0BR0...

Page 237 TMP91C824 Table 5.3 Address Map SFRs [11] WDT [12] RTC Address Address Name Name 0300H WDMOD 0320H SECR 1H WDCR 1H MINR 2H HOURR 3H DAYR 4H DATER 5H MONTHR 6H YEARR 7H PAGER 8H RESTR [13] MLD [14] MMU Address Address Name...

Page 238 TMP91C824 (1) I/O ports Symbol Name Address Port 1 Data from external port (Output latch register cleared to “0”.) Port 2 Data from external port (Output latch register is set to “1”.) Port 5 0 (Output latch register) : Pull-up resistor OFF 1 (Output latch register) : Pull-up resistor ON Port 6...

Page 239 TMP91C824 (2) I/O port control (1/2) Symbol Name Address P17C P16C P15C P14C P13C P12C P11C P10C Port 1 P1CR (Prohibit control RMW) 0: Input 1: Output P27F P26F P25F P24F P23F P22F P21F P20F Port 2 P2FC (Prohibit function RMW) 0: Port 1: Address bus (A23 to A16)

Page 240 TMP91C824 (2) I/O port control (2/2) Symbol Name Address ODEP72 ODEP71 Port 7 P7ODE open (Prohibit drain 0: 3 states RMW) 1: Open drain PB6C PB5C PB4C PB3C PB2C PB1C PB0C Port B PBCR (Prohibit control RMW) 0: Input 1: Output PB6F PB5F PB4F...

Page 241 TMP91C824 (3) Interrupt control (1/3) Symbol Name Address INTAD INT0 INT0 IADC IADM2 IADM1 IADM0 I0M2 I0M1 I0M0 INTE0AD INTAD enable 1: INTAD Interrupt level 1: INT0 Interrupt level INT2 INT1 INT1 I2M2 I2M1 I2M0 I1M2 I1M1 I1M0 INTE12 INT2 enable 1: INT2 Interrupt level...

Page 242: Interrupt Control

TMP91C824 (3) Interrupt control (2/3) Symbol Name Address INTTX0 INTRX0 INTTX0 ITX0C

ITX0M2 ITX0M1 ITX0M0 IRX0C IRX0M2 IRX0M1 IRX0M0 INTES0 INTTRX0 enable 1: INTTX0 Interrupt level 1: INTRX0 Interrupt level INTTX1 INTRX1 INTTX1 ITX1C ITX1M2 ITX1M1 ITX1M0 IRX1C IRX1M2 IRX1M1 IRX1M0 INTES1 INTTRX1...

Page 243 TMP91C824 (3) Interrupt control (3/3) Symbol Name Address DMA0V5 DMA0V4 DMA0V3 DMA0V2 DMA0V1 DMA0V0 DMA 0 DMA0V request vector DMA0 start vector DMA1V5 DMA1V4 DMA1V3 DMA1V2 DMA1V1 DMA1V0 DMA 1 DMA1V request vector DMA1 start vector DMA2V5 DMA2V4 DMA2V3 DMA2V2 DMA2V1 DMA2V0 DMA 2...

Page 244 TMP91C824 (4) Chip select/wait control (1/2) Symbol Name Address B0OM1 B0OM0 B0BUS B0W2 B0W1 B0W0 Block 0 CS/WAIT B0CS 0: Disable 00: ROM/SRAM Data bus 000: 2 waits 100: Reserved control (Prohibit 1: Enable width 001: 1 wait 101: 3 waits register 010: (1 + N) waits 110: 4 waits RMW)

Page 245 TMP91C824 (4) Chip select/wait control (2/2) Symbol Name Address Memory start MSAR2 address register 2 Start address A23 to A16 Memory address MAMR2 mask register 2 CS2 area size 0: Enable to address comparison Memory start MSAR3 address register 3 Start address A23 to A16 Memory address...

Page 246 TMP91C824 (5) Clock gear (1/2) Symbol Name Address XTEN RXEN RXTEN RSYSCK WUEF PRCK1 PRCK0 High- Low- High- Low- Select Warm-up Select prescaler clock 00: f frequency frequency frequency frequency clock after timer oscillator (fc) oscillator (fs) oscillator (fc) oscillator (fs) release of 0 write: 01: Reserved...

Page 247 TMP91C824 (5) Clock gear (2/2) Symbol Name Address − − − − EXTIN DRVOSCL PROTECT DRVOSCH Protection Always Always Always Always 1: External fc oscillator fs oscillator EMCCR0 control flag write 0 write 1 write 0 write 0 drivability driver register 0 0: OFF 1: Normal...

Page 248 TMP91C824 (6) DFM (Clock doubler) Symbol Name Address ACT1 ACT0 DLUPFG DLUPTM Lockup flag Lockup time DFMCR0 control 0: 2 0: End LUP 00 STOP STOP f OSCH OSCH register 0 1: 2 1: Do not 01 RUN OSCH OSCH 10 RUN STOP f 11 RUN STOP f OSCH...

Page 249 TMP91C824 (7) 8-bit timer (7−1) TMRA01 Symbol Name Address TA0RDE I2TA01 TA01PRUN TA1RUN TA0RUN 8-bit timer TA01RUN 100H IDLE2 8-bit timer run/stop control Double buffer register 0: Disable 0: Stop 0: Stop and clear 1: Enable 1: Operate 1: Run (Count up) −...

Page 250 TMP91C824 (8) UART/serial channel (1/2) (8-1) UART/SIO channel 0 Symbol Name Address Serial 200H RB7/TB7 RB6/TB6 RB5/TB5 RB4/TB4 RB3/TB3 RB2/TB2 RB1/TB1 RB0/TB0 SC0BUF channel 0 (Prohibit R (Receiving)/W (Transmission) buffer RMW) Undefined EVEN OERR PERR FERR SCLKS R (Cleared to 0 by reading) Serial Undefined SC0CR...

Page 251 TMP91C824 (8) UART/serial channel (2/2) (8-3) UART/SIO channel1 Symbol Name Address Serial 208H RB7/TB7 RB6/TB6 RB5/TB5 RB4/TB4 RB3/TB3 RB2/TB2 RB1/TB1 RB0/TB0 SC1BUF channel 1 (Prohibit R (Receiving)/W (Transmission) buffer RMW) Undefined EVEN OERR PERR FERR SCLKS R (Cleared to 0 by reading) Serial Undefined SC1CR...

Page 252 TMP91C824 (9) I C bus/serial interface Symbol Name Address SCK0/ 240H SCK2 SCK1 SWRMON C bus mode) Number of transfer bits Acknowledge Setting for the devisor value n 000: 8, 001: 1, 010: 2 mode 000: 4, 001: 5, 010: 6 (Prohibit 011: 3, 100: 4, 101: 5...

Page 253 TMP91C824 (10) AD converter Symbol Name Address − − EOCF ADBF ITM0 REPEAT SCAN 2B0H ADMOD0 MODE Always Always Interrupt in Repeat Scan mode register 0 conversion conversion write 0 write 0 repeat conversion mode specification end flag burst flag mode Star specification...

Page 254 TMP91C824 (11) Watchdog timer Symbol Name Address − WDTE WDTP1 WDTP0 I2WDT RESCR WDMOD mode 300H 00: 2 1: WDT IDLE2 1: RESET Always register 01: 2 enable 0: Abort write 0 10: 2 1: Operate 11: 2 − 301H WDCR (Prohibit −...

Page 255 TMP91C824 (12) RTC (Real time clock) Symbol Name Address Second SECR 320H register Undefined 0 is read 40 s 20 s 10 s Minute MINR 321H register Undefined 0 is read 40

min 20 min 10 min 8 min 4 min 2 min 1min Hour...

Page 256 TMP91C824 (13) Melody/alarm generator Symbol Name Address Alarm pattern 330H register Alarm pattern set − − − − ALMINV MELALM Melody/ Free-run counter Alarm Always write 0 Output 331H alarm MELALMC control frequency frequency control 00: Hold invert 0: Alarm register 01: Restart 1: Invert...

Page 257 TMP91C824 (14) MMU Symbol Name Address L0EA22 L0EA21 L0EA20 LOCAL0 control 350H LOCAL0 BANK for LOCAL0 area BANK set register LOCAL0 0: Disable “000” setting is prohibited because 1: Enable it pretend COMMON 0 area L1EA23 L1EA22 L1EA21 LOCAL1 control 351H LOCAL1 BANK for...

Page 258 TMP91C824 Points of Note and Restrictions (1) Notation The notation for built-in I/O registers is as follows register symbol <Bit symbol> e.g.) TA01RUN<TA0RUN> denotes bit TA0RUN of register TA01RUN. Read-modify-write instructions An instruction in which the CPU reads data from memory and writes the data to the same memory location in one instruction.

Page 259 TMP91C824 (2) Points of note AM0 and AM1 pins This pin is connected to the VCC or the VSS pin. Do not alter the level when the pin is active. EMU0 and EMU1 Open pins. Reserved address areas The TMP91C824 does not have any reserved areas. d.

Page 260 TMP91C824 m. Releasing the HALT mode by requesting an interruption Usually, interrupts can release all halts status. However, the interrupts (, INT0 to INT3, INTRTC, INTALM0 to INTALM4) which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f) with IDLE1 or STOP mode (IDLE2 is not applicable to this case).

Page 261: Package Dimensions

TMP91C824 Package Dimensions LQFP100-P-1414-0.50F Unit: mm 91C824-259 2008-02-20...

This manual is also suitable for:

Tmp91c824fgjtmp91c824-s