Asus Aaeon BOXER-6403WT User Manual

Fanless embedded box pc

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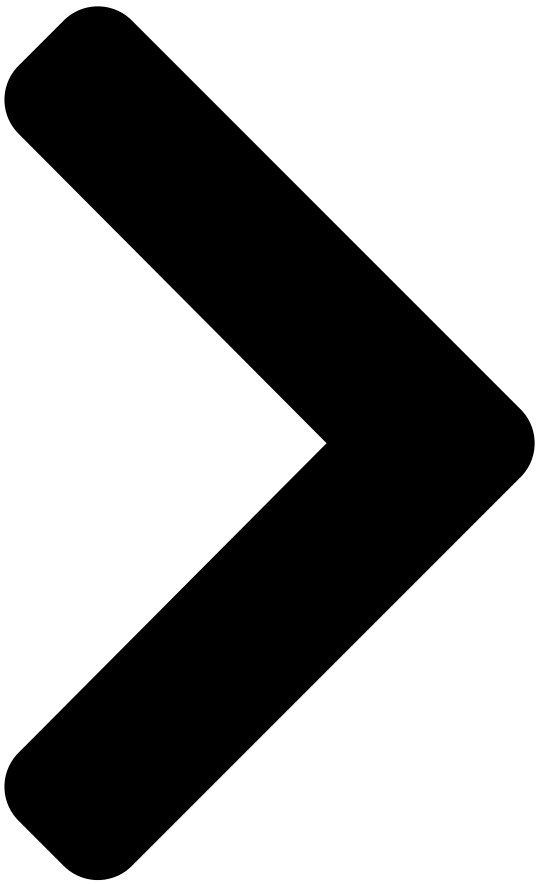

BOXER-6403WT

Fanless Embedded Box PC

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User's Manual 1

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Last Updated: March 25, 2016

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Related Manuals for Asus Aaeon BOXER-6403WT

Touch Panel Asus AAEON OMNI-ADP-KIT Series User Manual

Modular touch panel solutions (157 pages)

Touch Panel Asus AIO User Manual

(36 pages)

Touch Panel Asus AAEON ACP-1074 User Manual

(96 pages)

Touch Panel Asus AAEON OMNI-2155-CML User Manual

Industrial touch panel with 10th generation intel core processors (103 pages)

Touch Panel Asus AAEON ACP-1104 User Manual

Infotainment multi-touch panel pc (91 pages)

Summary of Contents for Asus Aaeon BOXER-6403WT

Page 1 BOXER-6403WT Fanless Embedded Box PC User’s Manual 1 Last Updated: March 25, 2016...

Page 2 Copyright Notice This document is copyrighted, 2016. All rights are reserved. The original manufacturer reserves the right to make improvements to the products described in this manual at any time without notice. No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means without the prior written permission of the original manufacturer.

Page 3 Acknowledgement All other products’ name or trademarks are properties of their respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. Intel, Pentium, Celeron, and Xeon are registered trademarks of Intel Corporation Atom is a trademark of Intel Corporation ...

Page 4 Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity BOXER-6403WT Burn-proof bracket RJ-45 to D-sub cable Power adapter Product DVD with User’s Manual (in pdf) and drivers ...

Page 5 About this Document This User’s Manual contains all the essential information, such as detailed descriptions and explanations on the product’s hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the AAEON.com for the latest version of this document.

Page 6 Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale.

Page 7 As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers. If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii.

Page 8 FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Page 9 China RoHS Requirements (CN) 产品中有毒有害物质或元素名称及含量 AAEON Embedded Box PC/ Industrial System 有毒有害物质或元素 部件名称 铅 汞 镉 六价铬 多溴联苯 多溴二苯醚 (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) 印刷电路板 ○ ○ ○ ○ ○ ○ 及其电子组件 外部信号 ○ ○ ○ ○ ○ ○ 连接器及线材...

Page 10 China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Embedded Box PC/ Industrial System Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) PCB &...

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Chapter 1 Chapter 1 - Product Specifications...

Page 15: Specifications

Specifications ® ® Intel Celeron /Atom Processor Processor DDR3L 1333 MHz SODIMM x 1, up to 8 GB System Memory ® Intel Atom™ E3845 Chipset   Display HDMI Interface DVI-D x 1 VGA x 1 Others 18/24-bit single channel Onboard LVDS x 1 (internal) Storage CF-SATA...

Page 16 Audio KB/MS Others Lockable DC Jack x 1, HDMI x 1 Expansion PCIe – – MiniCard Half-size MiniCard (mSATA only) x 1 Full-size MiniCard w/ SIM slot x 1 Mini PCI – Others Onboard USB Pin header x 1 Indicator Front –...

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List of Jumpers Please refer to the table below for all of the system’s jumpers that you can configure for your application Label Function AT/ATX Mode Selection LVDS BKLT Control Selection LVDS Power Selection LVDS BKLT Control Selection Clear CMOS Jumper Dry and Wet Contact Digital Input Power Selection Dry and Wet Contact Digital Output Power Selection Chapter 2 –...

Page 21: At/Atx Mode Selection (Jp1)

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Page 23: List Of Connectors

List of Connectors Please refer to the table below for all of the system's connectors that you can configure for your application Label Function HDMI Display USB 3.0 Connector COM2 RS-232/422/485 CN11 LPC Expansion I/F CN16 COM3 RS-232 I/F CN17 COM1 RS-232/422/485 CN22 BIOS SPI Flash Header...

Page 24: Hdmi Display (Cn1)

2.3.1 HDMI Display (CN1) Pin Name Signal Type Signal Level HDMI_TX2+ DIFF HDMI_TX2- DIFF HDMI_TX1+ DIFF HDMI_TX1- DIFF HDMI_TX0+ DIFF HDMI_TX0- DIFF HDMI_CLK+ DIFF HDMI_CLK- DIFF HDMI_DDC_CLK HDMI_DDC_DATA HDMI_PWR HDMI_HPD Chapter 2 – Hardware Information...

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Page 26: Lpc Expansion I/F (Cn11)

2.3.4 LPC Expansion I/F (CN11) Pin Name Signal Type Signal Level LAD0 +3.3V LAD1 +3.3V LAD2 +3.3V LAD3 +3.3V +3.3V +3.3V LFRAME# LRESET# +3.3V LCLK LDRQ0 LDRQ1 SERIRQ +3.3V 2.3.5 COM3 RS-232 I/F (CN16) Chapter 2 – Hardware Information...

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2.3.9 RJ-45 Ethernet Port (CN26) Pin Name Signal Type Signal Level MDI0+ DIFF MDI0- DIFF MDI1+ DIFF MDI2+ DIFF MDI2- DIFF MDI1- DIFF MDI3+ DIFF MDI3- DIFF 2.3.10 RJ-45 Ethernet Port (CN27) Pin Name Signal Type Signal Level MDI0+ DIFF MDI0- DIFF MDI1+...

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Page 34 mSATA RX+ DIFF +3.3V +3.3V mSATA RX- DIFF +1.5V +1.5V SMB_CLK +3.3V mSATA_TX DIFF SMB_DATA +3.3V mSATA_TX+ DIFF +3.3V +3.3V +3.3V +3.3V +1.5V +1.5V Chapter 2 – Hardware Information...

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Page 36 PCIE RX- DIFF +3.3V +3.3V PCIE RX+ DIFF +1.5V +1.5V SMB_CLK +3.3V PCIE TX DIFF SMB_DATA PCIE TX+ DIFF +3.3V +3.3V +3.3V +3.3V Chapter 2 – Hardware Information...

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Page 38: Chapter 3 - Ami Bios Setup

Chapter 3 Chapter 3 - AMI BIOS Setup...

Page 39: System Test And Initialization

System Test and Initialization The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors. The system configuration verification routines check the current system configuration against the values stored in the CMOS memory.

Page 40: Ami Bios Setup

AMI BIOS Setup The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off. To enter BIOS Setup, press <Del>...

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3.4.1 Advanced: CPU Configuration Options summary: Intel Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default EIST Disabled Enabled Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

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3.4.4 Advanced: Hardware Monitor Chapter 3 – AMI BIOS Setup...

Page 47: Advanced: Dynamic Digital Io Configuration

3.4.5 Advanced: Dynamic Digital IO Configuration Options summary: GPO0 Direction [Output] Output Level Optimal Default, Failsafe Default GPO1 Direction [Output] Output Level Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

Page 48: Advanced: Power Management

3.4.6 Advanced: Power Management Options summary: Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select power supply mode. AC Power Loss Last State Optimal Default, Failsafe Default Power On Power Off Select power state when power is re-applied after a power failure. RTC wake system Disabled Optimal Default, Failsafe Default...

Page 49: Advanced: Sio Configuration

3.4.7 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

Page 50: Sio Configuration: Serial Port 1 Configuration

3.4.7.1 SIO Configuration: Serial Port 1 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=3F8; IRQ=4; IO=2F8; IRQ=3; Select an optimal setting for IO device Mode: RS232 Optimal Default, Failsafe Default...

Page 51: Sio Configuration: Serial Port 2 Configuration

3.4.7.2 SIO Configuration: Serial Port 2 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2F8; IRQ=3; IO=3F8; IRQ=4; Select an optimal setting for IO device Mode: RS232 Optimal Default, Failsafe Default...

Page 52: Sio Configuration: Serial Port 3 Configuration

3.4.7.3 SIO Configuration: Serial Port 3 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=3E8; IRQ=11; IO=2E8; IRQ=11; Select an optimal setting for IO device Chapter 3 –...

Page 53: Setup Submenu: Chipset

Setup submenu: Chipset Chapter 3 – AMI BIOS Setup...

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3.5.1 Chipset: North Bridge Chapter 3 – AMI BIOS Setup...

Page 55: Display Control Configuration

3.5.1.1 Display Control Configuration Options summary: DVMT Pre-Allocated Optimal Default, Failsafe Default 128M 160M 192M 224M 256M 288M 320M 352M 384M 416M 448M 480M 512M DVMT Total Gfx Mem 128MB Chapter 3 – AMI BIOS Setup...

Page 56 256MB Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

Page 57: South Bridge

3.5.2 South Bridge Options summary: Audio Controller Disabled Enabled Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

Page 58: Security

Security Change User/Administrator Password You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility. Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers).

Page 59 Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection. Chapter 3 – AMI BIOS Setup...

Page 60: Setup Submenu: Boot

Setup submenu: Boot Options summary: Quiet Boot Disabled Enabled Default En/Disable showing boot logo. Option ROM Messages Force BIOS Default Keep Current Set display mode for Option ROM Launch PXE OpROM Disabled Default Enabled En/Disable Legacy Boot Option Chapter 3 – AMI BIOS Setup...

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Setup submenu: Exit Chapter 3 – AMI BIOS Setup...

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Chapter 4 Chapter 4 – Drivers Installation...

Page 64: Product Cd/Dvd

Product CD/DVD The BOXER-6403WT comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers. In case the program does not start, follow the sequence below to install the drivers. Step 1 –...

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Step 4 – Install xHCI Driver (Windows 7 only) Open the Step 4 - xHCI folder and followed by the Setup.exe file Follow the instructions Drivers will be installed automatically Step 5 – Install Intel Sideband Fabric Device Drivers (Windows 8.1 only) Open the Step 5 - Intel Sideband Fabric Device followed by the Setup.exe file Follow the instructions...

Page 66: Appendix A - Watchdog Timer Programming

Appendix A Appendix A - Watchdog Timer Programming...

Page 67: Watchdog Timer Initial Program

A.1 Watchdog Timer Initial Program Table 1 : SuperIO relative register table Default Value Note SIO MB PnP Mode Index Register Index 0x2E(Note1) 0x2E or 0x4E SIO MB PnP Mode Data Register Data 0x2F(Note2) 0x2F or 0x4F Table 2 : Watchdog relative register table Register BitNum Value...

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********** // SuperIO relative definition (Please reference to Table 1) #define byte SIOIndex //This parameter is represented from Note1 #define byte SIOData //This parameter is represented from Note2 #define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte IOPort); // Watch Dog relative definition (Please reference to Table 2) #define byte TimerLDN //This parameter is represented from Note3 #define byte TimerReg //This parameter is represented from Note4 #define byte TimerVal // This parameter is represented from Note24...

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********** VOID Main(){ // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) // (boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure : AaeonWDTEnable // This procudure will enable the WDT counting. AaeonWDTEnable(); ********** Appendix A – Watchdog Timer Programming...

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********** // Procedure : AaeonWDTEnable VOID AaeonWDTEnable (){ WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1); // Procedure : AaeonWDTConfig VOID AaeonWDTConfig (){ // Disable WDT counting WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0); // Clear Watchdog Timeout Status WDTClearTimeoutStatus(); // WDT relative parameter setting WDTParameterSetting(); VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){ SIOBitSet(LDN, Register, BitNum, Value);...

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********** VOID SIOEnterMBPnPMode(){ IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); VOID SIOExitMBPnPMode(){ IOWriteByte(SIOIndex, 0xAA); VOID SIOSelectLDN(byte LDN){

IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN); VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){ Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData);...

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Appendix B Appendix B - I/O Information...

Page 73: I/O Address Map

I/O Address Map Appendix B – I/O Information...

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Memory Address Map Appendix B – I/O Information...

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Page 80: Appendix C - Electrical Specifications For I/O Ports

Appendix C Appendix C – Electrical Specifications for I/O Ports...

Page 81: Electrical Specifications For I/O Ports

Electrical Specifications for I/O Ports Reference Signal Name Rate Output Backlight +5V/0.5 or Brightness Control CN19 +VCC_LVDS_BKLT +12V/0.5 Connector Iternal LVDS +3.3V/1A or CN25 Connector +5V/1A HDMI Connector +5V/1A +5V/1Aer USB3.0 Connector USB3 channel) +3.3VSB +3.3V/1.1A mSATA Connector PCIE1_A1 +1.5V +1.5V/0.375A COM1 +5V/0.5A or...

Page 82: Appendix D - Digital I/O Ports

Appendix D Appendix D – Digital I/O Ports...

Page 83: Di/O Programming

DI/O Programming The BOXER-6403WT utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application. There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode (2) Modify the data of configuration registers (3) Exit the MB PnP Mode.

Page 84: Digital I/O Register

Digital I/O Register Table 2 : SuperIO relative register table Default Value Note SIO MB PnP Mode Index Register Index 0x2E 0x2E or 0x4E SIO MB PnP Mode Data Register Data 0x2F) 0x2F or 0x4F Table 2 : Digital Input relative register table Register BitNum Value...

Page 85: Digital I/O Sample Program

Digital I/O Sample Program ********** // SuperIO relative definition (Please reference to Table 1) #define byte SIOIndex //This parameter is represented from Note1 #define byte SIOData //This parameter is represented from Note2 #define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte IOPort); // Digital Input Status relative definition (Please reference to Table 2) #define byte DInput1LDN // This parameter is represented from Note3 #define byte DInput1Reg // This parameter is

represented from Note4...

Page 86 ********** // Digital Output control relative definition (Please reference to Table 3) #define byte DOutput1LDN // This parameter is represented from Note21 #define byte DOutput1Reg // This parameter is represented from Note22 #define byte DOutput1Bit // This parameter is represented from Note23 #define byte DOutput1Val // This parameter is represented from Note24 #define byte DOutput2LDN // This parameter is represented from Note25 #define byte DOutput2Reg // This parameter is represented from Note26...

Page 87 ********** VOID Main(){ Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin level is High PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit); // Procedure : AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...

Page 88 ********** Boolean AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){ Boolean PinStatus ; PinStatus = SIOBitRead(LDN, Register, BitNum); Return PinStatus ; VOID AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){ ConfigToOutputMode(LDN, Register, BitNum); SIOBitSet(LDN, Register, BitNum, Value); ********** Appendix D – Digital I/O Ports...

Page 89 ********** VOID SIOEnterMBPnPMode(){ IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); VOID SIOExitMBPnPMode(){ IOWriteByte(SIOIndex, 0xAA); VOID SIOSelectLDN(byte LDN){ IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN); VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){ Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData);...

Page 90 ********** Boolean SIOBitRead(byte LDN, byte Register, byte BitNum){ Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(LDN); IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData); TmpValue &= (1 << BitNum); SIOExitMBPnPMode(); If(TmpValue == 0) Return 0; Return 1; VOID ConfigToOutputMode(byte LDN, byte Register, byte BitNum){ Byte TmpValue, OutputEnableReg; OutputEnableReg = Register-1;...