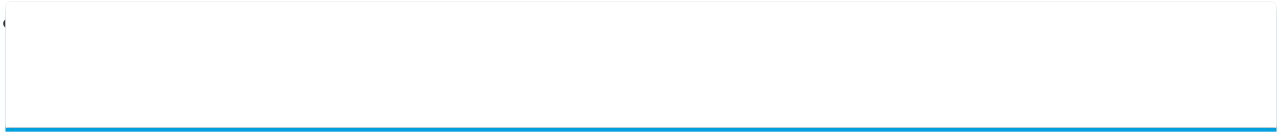
Asus AAEON COM-BYTC2 User Manual

Com express module

1
2
3
4
5
6
7
8
9
10
Table Of Contents
11
12
13
14
15
16
17

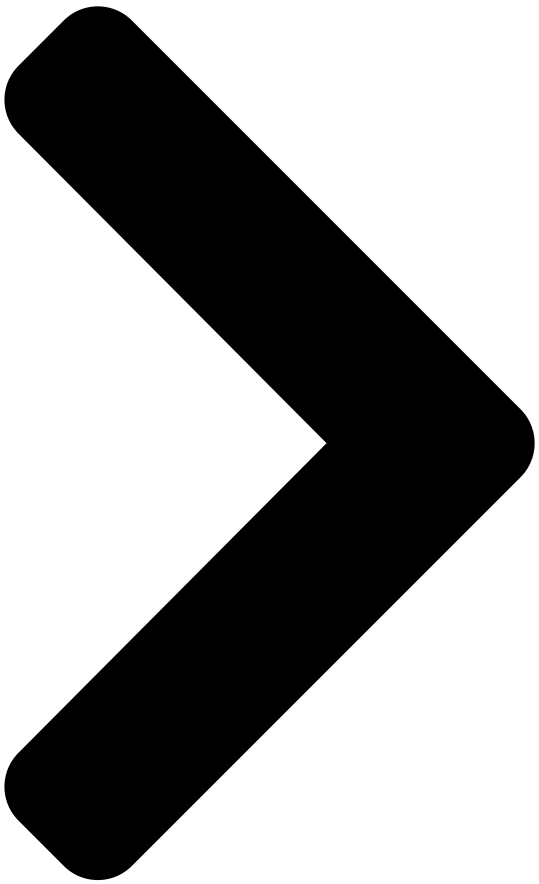


-

Table of Contents

-

Bookmarks



COM-BYTC2

COM Express Module

User 's Manual 3rd Ed

Last Updated: October 12, 2021

Table of Contents

Next Page

Related Manuals for Asus AAEON COM-BYTC2

Control Unit Asus Aaeon COM-SKUC6 User Manual

Com express module (99 pages)

Control Unit Asus AAEON COM-SKUC6 User Manual

Com express module (100 pages)

Control Unit Asus AAEON COM-WHUC6 User Manual

Com express module (110 pages)

Control Unit Asus AAEON COM-BT-A30 User Manual

Com express module (98 pages)

Control Unit Asus AAEON COM-TGHB6 User Manual

(88 pages)

Control Unit Asus AAEON COM-SKHB6 User Manual

(76 pages)

Control Unit Asus AAEON COM-TGUC6 User Manual

Com express module (103 pages)

Control Unit Asus AAEON COM-ADNC6 User Manual

Com express module (89 pages)

Control Unit Asus Aaeon NanoCOM-APL User Manual

Com express module (77 pages)

Control Unit Asus ThunderboltEX 3-TR User Manual

(14 pages)

Control Unit Asus TPM-SPI Quick Start Manual

14-1 pin (4 pages)

Control Unit Asus AAEON MXM-ACMA User Manual

(26 pages)

Control Unit Asus AAEON MIPICSI Camera RVP Converter Kit User Manual

Up expansion module (47 pages)

Control Unit Asus Aaeon NanoCOM-TGU User Manual

Com express module (95 pages)

Control Unit Asus AAEON ASDM-L-CFS User Manual

Smart display module (82 pages)

Control Unit Asus Aaeon NIM-S26B Quick Installation Manual

Network interface module (23 pages)

Summary of Contents for Asus AAEON COM-BYTC2

Page 1 COM-BYTC2 COM Express Module User ’s Manual 3 Last Updated: October 12, 2021...

Page 2 Copyright Notice This document is copyrighted, 2021. All rights are reserved. The original manufacturer reserves the right to make improvements to the products described in this manual at any time without notice. No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means witho ut the prior written permission of the original manufacturer.

Page 3 Acknowledgements All other products’ name or trademarks are properties of their

respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. ● Intel®, Pentium®, Celeron®, and Xeon® are registered trademarks of Intel ● Corporation Intel Core™ and Intel Atom™ are trademarks of Intel Corporation ●...

Page 4 Packing List Before setting up your product, please make sure the following items have been shipped: I t em Quantity COM-BYTC2 ● If any of these items are missing or damaged, please contact your distributor or sales representative immediately. Preface...

Page 5 About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the product page at AAEON.com for the latest version of this document.

Page 6 Saf e ty Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

Page 7 If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

Page 8 FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Page 9 Chi na RoHS Requirements (CN) □□□□□□□□□□□□□□□□□ AAEON Main Board/ Daughter Board/ Backplane □□□□□□□□□ □□□□ □ □ □ □□□ □□□□ □□□□□ (Pb) (Hg) (C d) (C r(VI)) (PBB) (PBDE) □□ □□□ ○ ○ ○ ○ ○ ○ □□□□□□ □□□□ ○ ○ ○...

Page 10 Chi na RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Main Board/ Daughter Board/ Backplane Poisonous or Hazardous Substances or Elements He xavalent Polybrominated Polybrominated C omponent Le ad Me rcury C admium C hromium Biphenyls Diphenyl Ethers (Pb) (Hg)

Page 11: Table Of Contents

Table of Contents Chapter 1 - Product Specifications.....1 Specifications .....

Page 12 3.4.6 Advanced: CSM Configuration.....33 3.4.7 Advanced: SIO Configuration .....34 3.4.8 Advanced: Serial Port Configuration .....35 Setup submenu: Chipset .....36 3.5.1 Chipset: North Bridge Configuration.....37 3.5.1.1 North Bridge Configuration: Display Control Config uration .....38 3.5.2 Chipset: South Bridge Configuration .....41 Setup submenu: Security .....

Page 13: Chapter 1 - Product Specifications

Chapter 1 Chapter 1 - Product Specifications...

Page 14: Specifications

1 .1 Spe cifications System F o rm Factor COM Express Compact Size, Type 2 CP U Intel® Atom™/ Celeron® Processor CP U Frequency Up to 1.91 GHz, J1900 Chip set Intel® Atom™/ Celeron® SoC Memory Type DDR3L 1333, SODIMM x 1 Max.

Page 15 Et hernet Intel® i210IT Gigabit Ethernet x 1 A ud io High Definition Audio Interface U SB Port USB2.0 x 7 Serial Port — HDD Interface SATA II x 1 PATA x 1 Exp ansion PCIe [x1] x 2 (up to 2 devices) PCI x 4 SMBus GP IO...

Page 16: Chapter 2 - Hardware Information

Chapter 2 Chapter 2 – Hardware Information...

Page 31: Backlight (Cn4)

P in P in Name Sig nal Type BKLT_EN_3.3S EPC_HPD +VLED +VLED +VLED +VLED 2.3.4 Backlight (CN4) P in P in Name Sig nal Type +VLED BKL_CTRL_3.3S BKL_EN_3.3S Chapter 2 – Hardware Information...

Page 32: Spi Flash Tool (Cn5)

2.3.5 SPI FL ASH tool (CN5) P in P in Name Sig nal Type SPI_SO_F SPI_CLK_F +V3.3A_SPI SPI_SI_F SPI_CE0#_F 2.3.6 LPC (CN6) P in P in Name Sig nal Type LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 +V3.3S LPC_FRAME# BUF_PLT_RST# PCI_CLK_SIO INT_SERIRQ_3P3 Chapter 2 –...

Page 33: Rtc Battery (Bat1)

2.3.7 RTC Battery (BAT1) P in P in Name Sig nal Type +V3.3A_RTC Chapter 2 – Hardware Information...

Page 34: List Of Leds

2.4 Li st of LEDs Please refer to the table below for all of the board’s LEDs that you can find the status Lab el F unction LED1 SATA Detect LED2 (Blue) S0 Voltage LED3 (Red) S5 Voltage 2.5 Function Block Diagram Chapter 2 –...

Page 35: Chapter 3 - Ami Bios Setup

Chapter 3 Chapter 3 - AMI BIOS Setup...

Page 36: System Test And Initialization

System Test and Initialization The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors. The system configuration verification routines check the current system configuration against the values stored in the CMOS memory.

Page 37: Ami Bios Setup

3.2 AMI BIOS Setup The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off. To enter BIOS Setup, press <Del>...

Page 38: Setup Submenu: Main

3.3 Se tup submenu: Main Press Delete to enter Setup Chapter 3 – AMI BIOS Setup...

Page 39: Setup Submenu: Advanced

3.4 Se tup submenu: Advanced Chapter 3 – AMI BIOS Setup...

Page 40: Advanced: Cpu Configuration

3.4.1 Advanced: CPU Configuration Options summary: Intel Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default EIST Disabled Optimal Default, Failsafe Default Enabled Chapter 3 – AMI BIOS Setup...

Page 41: Advanced: Ide Configuration (Ide)

3.4.2 Advanced: IDE Configuration (IDE) Options summary: SATA Mode IDE Mode AHCI Mode Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

Page 42: Advanced: Usb Configuration

3.4.3 Advanced: USB Configuration Options summary: Legacy USB Support Enabled Optimal Default, Failsafe Default Disabled Auto Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected Device Name (Emulation Auto Optimal Default, Failsafe Default...

Page 43: Advanced: On-Module H/W Monitor

3.4.4 Advanced: On-Module H/W Monitor Chapter 3 – AMI BIOS Setup...

Page 44: Advanced: Power Management

3.4.5 Advanced: Power Management Options summary: Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select power supply mode. Restore on Power Last State Loss Power On Power Off Optimal Default, Failsafe Default Select power state when power is re-applied after a power failure. RTC wake system Disabled Optimal Default, Failsafe Default...

Page 45: Advanced: Csm Configuration

3.4.6 Advanced: CSM Configuration Options summary: CSM Support Disabled Enabled Optimal Default, Failsafe Default Enable/Disable CSM Support Storage Do not launch UEFI Legacy Optimal Default, Failsafe Default Controls the execution of UEFI and Legacy storage OpROM Video Do not launch UEFI Legacy Optimal Default, Failsafe Default...

Page 46: Advanced: Sio Configuration

3.4.7 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

Page 47: Advanced: Serial Port Configuration

3.4.8 Advanced: Serial Port Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2D8; IRQ=11; IO=2C8; IRQ=11; Select an optimal setting for IO device Chapter 3 – AMI BIOS Setup...

Page 48: Setup Submenu: Chipset

3.5 Se tup submenu: Chipset Chapter 3 – AMI BIOS Setup...

Page 49: Chipset: North Bridge Configuration

3.5.1 Chi pset: North Bridge Configuration Chapter 3 – AMI BIOS Setup...

Page 50 3.5.1.1 Nor th Bridge Configuration: Display Control Configuration Options summary: DVMT Pre-Allocated Optimal Default, Failsafe Default 128M 160M ... 512M DVMT Total Gfx Mem 128MB 256MB Optimal Default, Failsafe Default Primary IGFX Boot VBIOS Default Optimal Default, Failsafe Default Display LVDS DP/HDMI Chapter 3 –...

Page 51 Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display Secondary IGFX Boot Disabled Optimal Default, Failsafe Default Display...

Page 52 Chapter 3 – AMI BIOS Setup...

Page 53: Chipset: South Bridge Configuration

3.5.2 Chi pset: South Bridge Configuration Options summary: Audio Controller Enabled Optimal Default, Failsafe Default Disabled Chapter 3 – AMI BIOS Setup...

Page 54: Setup Submenu: Security

3.6 Se tup submenu: Security Change User/Administrator Password Y ou can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Page 55: Setup Submenu: Boot

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection. 3.7 Se tup submenu: Boot Options summary: Quiet Boot Disabled Enabled Default En/Disable showing boot logo. Option ROM Messages Force BIOS Default Keep Current Set display mode for Option ROM...

Page 56

This option controls Legacy/UEFI ROMs priority Chapter 3 – AMI BIOS Setup...

Page 57: Boot: Hard Drive Bbs Priorities

3.7.1 Boot: Hard Drive BBS Priorities Chapter 3 – AMI BIOS Setup...

Page 58: Setup Submenu: Save & Exit

3.8 Se tup submenu: Save & Exit Chapter 3 – AMI BIOS Setup...

Page 59: Chapter 4 - Drivers Installation

Chapter 4 Chapter 4 – Drivers Installation...

Page 60: Driver Download/Installation

Dri ver Download/Installation Drivers for the COM-BYTC2 can be downloaded from the product page on the AAEON website by following this link: https://www.aaeon.com/en/p/modulescom-express-modules-com-bytc2 Download the driver(s) you need and follow the steps below to install them . St ep 1 – Install Chipset Driver Open the St ep1 - Chipset folder followed by SetupChipset.exe Follow the instructions Drivers will be installed automatically...

Page 61

St ep 4 – Install xHCI Driver Open the STEP4 - xHCI folder followed by Set up.exe Follow the instructions Drivers will be installed automatically St ep 5 – Install Intel Sideband Fabric Device Driver Open the STEP5 –Intel Sideband Fabric Device folder followed by Setup.exe Follow the instructions Drivers will be installed automatically St ep 6 –...

Page 62: Appendix A - Watchdog Timer Programming

Appendix A Appendix A - Watchdog Timer Programming...

Page 63: Watchdog Timer Initial Program

Watchdog T imer Initial Program Tab le 1 : Embedded BRAM relative register table Default Value N o te I nd ex 0x284(Note1) BRAM Index Register Dat a 0x285(Note2) BRAM Data Register Lo g ical Device Number 0xA 8(Note3) Watch dog Logical Device Number F unction and Device Number 0x00(Note4) Watch dog Function/Device Number...

Page 64

********** // Embedded BRAM relative definition (Please reference to Table 1) #d efine byte EcBRAMIndex //This parameter is represented from N o te1 #d efine byte EcBRAMData //This parameter is represented from N ote2 #d efine byte BRAMLDNReg //This parameter is represented from N o te3 #d efine byte BRAMFnDataReg //This parameter is represented from N o te4 #d efine vo id EcBRAMWriteByte(byte Offset, b yte Value);...

Page 65

********** VOID Main(){ // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) // (boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure : AaeonWDTEnable // This procudure will enable the WDT counting. AaeonWDTEnable(); ********** Appendix A – Watchdog Timer Programming...

Page 66

********** // Procedure : AaeonWDTEnable VOID A aeonWDTEnable (){ WDTEnableDisable(1); // Procedure : AaeonWDTConfig VOID A aeonWDTConfig (){ // Disable WDT counting WDTEnableDisable(0); // WDT relative parameter setting WDTParameterSetting(); VOID W DTEnableDisable(byte Value){ ECBRAMWriteByte(TimerReg , Value); VOID W DTParameterSetting(){ Byte TempByte; // Watchdog Timer counter setting ECBRAMWriteByte(TimerReg , TimerVal);...

Page 67

********** VOID ECB RAMWriteByte(byte OPReg, byte OPBit, byte Value){ IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg); IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData, 0x30); //Write start Byte ECBRAMReadByte(byte OPReg){ IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);

IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x12);...

Page 68: Appendix B - I/O Information

Appendix B Appendix B - I/O Information...

Page 69: I/O Address Map

I/O Address Map Appendix B – I/O Informati o n...

Page 70

Appendix B – I/O Informati o n...

Page 71: Memory Address Map

B.2 Me m or y Address Map Appendix B – I/O Informati o n...

Page 72: Irq Mapping Chart

B.3 IRQ Mapping Chart Appendix B – I/O Informati o n...

Page 73

Appendix B – I/O Informati o n...

Page 74

Appendix B – I/O Informati o n...

Page 75

Appendix B – I/O Informati o n...

Page 76

Appendix B – I/O Informati o n...

Page 77

Appendix B – I/O Informati o n...

Page 78

Appendix B – I/O Informati o n...

Page 79

Appendix B – I/O Informati o n...

Page 80

Appendix B – I/O Informati o n...

Page 81

Appendix B – I/O Informati o n...

Page 82

Appendix B – I/O Informati o n...

Page 83

Appendix B – I/O Informati o n...

Page 84: Appendix C - Programming Digital I/O

Appendix C Appendix C – Programming Digital I/O...

Page 85: Digital I/O Register

Di gital I/O Register Tab le 1 : Embedded BRAM relative register table Default Value N o te I nd ex 0x284(Note1) BRAM Index Register Dat a 0x285(Note2) BRAM Data Register Lo g ical Device Number 0xA 2(Note3) Watch dog Logical Device Number I np ut/Output DIO Input/Output Function/Device 0x00(Note4)

Page 86: Digital I/O Sample Program

C.2 Di gital I/O Sample Program
********** //
Embedded BRAM relative definition (Please reference to Table 1) #d efine byte EcBRAMIndex //This parameter is represented from N o te1 #d efine byte EcBRAMData //This parameter is represented from N ote2 #d efine byte BRAMLDNReg //This parameter is represented from N o te3 #d efine byte BRAMFnData0Reg //This parameter is represented from N o te4 #d efine byte BRAMFnData1Reg //This parameter is represented from N o te5...

Page 87

****

VOID Main(){ Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin level is High PinStatus = AaeonReadPinStatus(DI O0ToDIO7Reg, DIO3Bit); // Procedure : AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...

Page 88 **********

Boolean A aeonReadPinStatus(byte OptionReg, byte BitNum) { Byte TempByte; TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg); If (TempByte & BitNum == 0) Return 0; Return 1; VOID A aeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){ Byte TempByte; TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg); TempByte |= (Value << BitNum); ECBRAMWriteByte(OptionReg, BitNum, Value);...

Page 89 **********

VOID ECB RAMWriteByte(byte OPReg, byte OPBit, byte Value){ IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg); IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData, 0x30); //Write start Byte ECBRAMReadByte(byte FnDataReg, byte OPReg){ IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, FnDataReg);...

Page 90: Appendix D -Notes For Users

Appendix D Appendix D –Notes for Users...

Page 91: Notes For Users

Note s for Users Please observe the following items to ensure optimal performance: eDP limitation Display Default: CRT + LVDS If you want to use the onboard eDP, please contact AAEON tech support for the BIOS that support onboard eDP. Due to the limitation, eDP works only on major OS and no display in DOS environment.