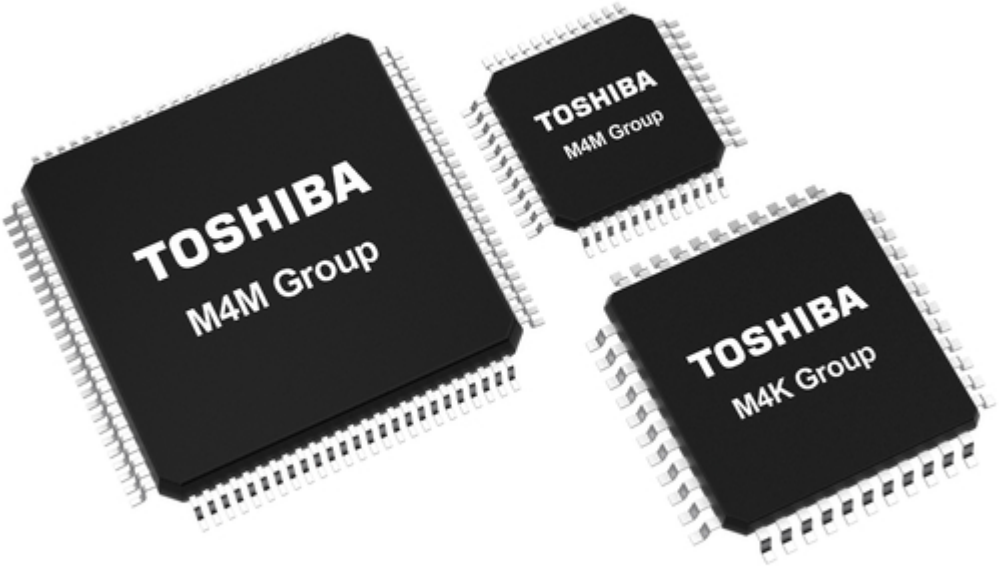
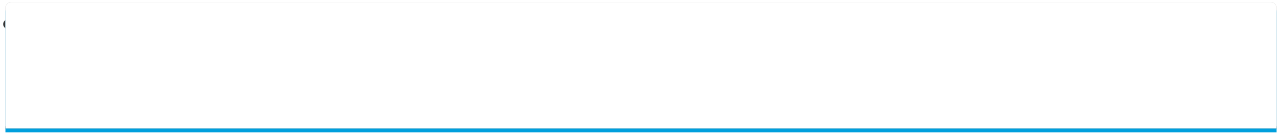

TOSHIBA
M4M Group
TOSHIBA
M4M Group
TOSHIBA
M4K Group

Toshiba TXZ+ Series Reference Manual

1
Table Of Contents
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17

68
69
70
71
72

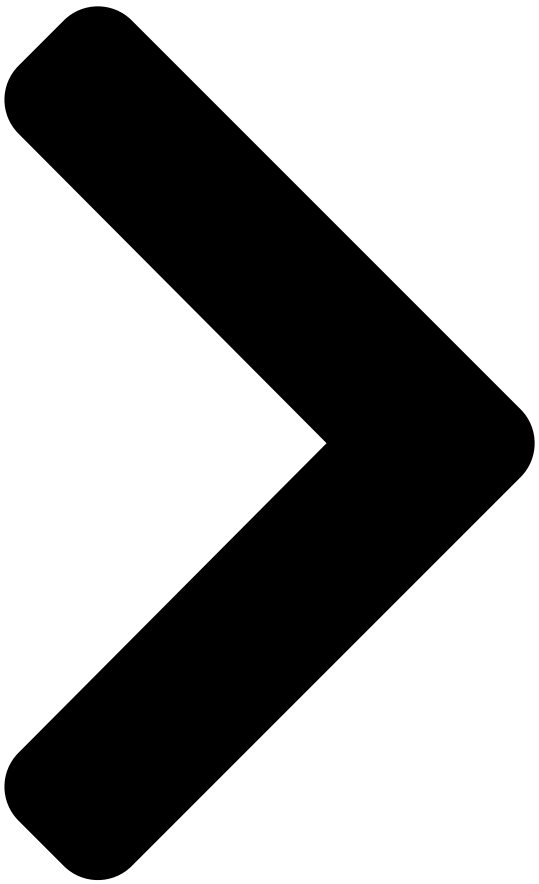


-

Table of Contents

-

Bookmarks



TXZ+ Family
TMPM3H Group(1)
Clock Control and Operation Mode

32-bit RISC Microcontroller

TXZ+ Family

TMPM3H Group(1)

Reference Manual

Clock Control and Operation Mode (CG-M3H(1)-D)

Revision 1.3

2022-05

2022-05-10

Toshiba Electronic Devices & Storage Corporation

Rev. 1.3

Table of Contents

Next Page

Related Manuals for Toshiba TXZ+ Series

Microcontrollers Toshiba TXZ+ Series Reference Manual

32-bit risc microcontroller, clock control and operation mode cg-m4g(1)-c (88 pages)

Microcontrollers Toshiba TXZ+ Series Reference Manual

2-bit risc microcontroller (64 pages)

Controller Toshiba TXZ+ Series Reference Manual

(52 pages)

Microcontrollers Toshiba TXZ+ TMPM3H Reference Manual

32-bit risc microcontroller (71 pages)

Microcontrollers Toshiba TXZ Family Reference Manual

32-bit risc microcontroller txz family reference manual comparator (comp-b) (15 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller, serial peripheral inteface tspi-b (67 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller (17 pages)

Microcontrollers TOSHIBA TXZ SERIES Reference Manual

Oscillation frequency detector (20 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller. can controller (can-a) (54 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller advanced encoder input circuit (32-bit) (55 pages)

Microcontrollers TOSHIBA TXZ Reference Manual

32-bit risc microcontroller (120 pages)

Microcontrollers Toshiba TX79 Series User Manual

Tx system risc symmetric 2-way superscalar 64-bit cpu (309 pages)

Microcontrollers Toshiba TX03 Series Manual

32 bit risc microcontroller (544 pages)

Microcontrollers Toshiba TXZ Plus Series Reference Manual

32-bit risc microcontroller (82 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Data Book

32bit micro controller (495 pages)

Microcontrollers Toshiba TMP96C141AF Manual

Cmos 16-bit microcontroller (178 pages)

Summary of Contents for Toshiba TXZ+ Series

Page 1 TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 32-bit RISC Microcontroller TXZ+ Family TMPM3H Group(1) Reference Manual Clock Control and Operation Mode (CG-M3H(1)-D) Revision 1.3 2022-05 © 2020-2022 2022-05-10 1 / 72 Toshiba Electronic Devices & Storage Corporation Rev. 1.3...

Page 2: Table Of Contents

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode Contents Contents .....2 List of Figures ..... 5 List to Tables 5

Preface ..... 6 Related documents .....6 Conventions .....7 Terms and Abbreviations .....9 Clock Control and Operation Mode .....10 1.1.

Page 3 TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.4.1. NORMAL → IDLE → NORMAL Operation mode transition ..... 33 1.3.4.2. NORMAL → STOP1 → NORMAL Operation mode transition .....33 1.3.4.3. NORMAL → STOP2 → RESET → NORMAL Operation mode transition .....34 1.4.

Page 4 TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.1.2. Reset by a RESET_N pin ..... 62 3.2.1.3. Continuation of reset by LVD .....64 3.2.2. Warm reset ..... 65 3.2.2.1. Warm reset by RESET_N pin .....65 3.2.2.2. Warm reset by internal reset .....65 3.2.3.

Page 5: List Of Figures

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode List of Figures Figure 1.1 Clock system diagram.....12 Figure 1.2 Mode State Transition .....26 Figure 1.3 STOP2 mode restart operation flow .....32 Figure 1.4 NORMAL → STOP1 → NORMAL Operation mode transition .....33 Figure 1.5 NORMAL →...

Page 6: Preface

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode Preface Related documents Document name ® ® Cortex -M3 Processor Technical Reference Manual The datasheet of each product (Electrical Characteristics) Exception Oscillation Frequency Detector Voltage Detection Circuit Clock Selective Watchdog Timer Flash Memory 2022-05-10 6 / 72...

Page 7: Conventions

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode Conventions ● Numeric formats follow the rules as shown below: Hexadecimal: 0xABC Decimal: 123 or 0d123 (Only when it needs to be explicitly shown that they are decimal numbers.) Binary: 0b111 (It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.) ●...

Page 8 TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode

Page 9: Terms And Abbreviations

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode Terms and Abbreviations Some of abbreviations used in this document are as follows: Analog to Digital Converter A-ENC Advanced Encoder input Circuit Advanced Peripheral Bus A-PMD Advanced Programmable Motor Control Circuit Clock control and Operation Mode COMP Comparator...

Page 10: Clock Control And Operation Mode

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1. Clock Control and Operation Mode 1.1. Outlines The clock/mode control block can select a clock gear and prescaler clock and set the warm up of oscillator and so Furthermore, it has NORMAL mode and a Low Power Consumption mode in order to reduce power consumption using mode transition.

Page 11: Clock Control

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2. Clock control 1.2.1. Clock type This section shows a list of clocks. EHCLKIN: The clock input from the external. A clock generated in the internal oscillation circuit or input from the X1 and X2 pins A clock multiplied by PLL A clock selected by [CGPLL0SEL]<PLL0SEL>...

Page 12: Clock System Diagram

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.3. Clock System diagram The figure below shows a clock system diagram. [CGWUPHCR]<WUON>

[CGWUPHCR]<WUPT[15:4]> [CGSPCLKEN] <ADCKEN> High Speed □ADC Warming up timer ADCLK [CGWUPHCR] <WUCLK> [CGFCEN]<FCIPEN07> [CGOSCCR]<IHOSC1EN> After reset :Oscillation □DNF Internal High Speed PLL for fsys...

Page 13: Warming Up Function

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.4. Warming up function A warming up function is used to secure the oscillation stable time at the time of the STOP1 mode release which starts the warming up timer for high speed oscillation automatically. It is available also as a count up timer which uses the exclusive warming up timer of high speed clock /each low speed clock for the waiting for the stability of an external oscillator or an internal oscillator.

Page 14: The Warming Up Timer For A Low Speed Oscillation

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.4.2. The warming up timer for a low speed oscillation A 19-bit up-timer is built in as a warming up timer only for a low speed oscillation. The setting value is calculated in the following formula, set [CGWUPLCR]<WUPT[18:4]>...

Page 15: Clock Multiplying Circuit (Pll) For Fsys

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.5. Clock multiplying circuit (PLL) for fsys The clock multiplying circuit outputs the fPLL clock (up to 120MHz) multiplied by the optimum condition for the frequency (6MHz to 12MHz) of the output clock fOSC of the high speed oscillator. So, it is possible to make the input frequency to an oscillator low speed and to make an internal clock high speed by this circuit.

Page 16

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode is denoted by the following formulas. × ([CGPLL0SEL]<PLL0SET[7:0]> + [CGPLL0SEL]<PLL0SET[11:8]>) × ([CGPLL0SEL] <PLL0SET[13:12]>) Note1. The absolute value of frequency accuracy is not guaranteed. Note2. There is no Linearity in the frequency by the fractional part Multiplication setup. ≤...

Page 17: Change Of The Pll Multiplication Value Under Operation

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.5.3. Change of the PLL multiplication value under operation It changes to a setup which sets "0" to [CGPLL0SEL]<PLL0SEL> first, and does not use a PLL multiplication clock during PLL multiplication clock operation when changing a multiplication value. And [CGPLL0SEL] <PLL0ST>...

Page 18: System Clock

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.6. System clock An internal high speed oscillation clock or external high speed oscillation clock (connected oscillator or clock input) can be used as a source of system clock. Dividing is possible for a system clock at [CGSYSCR]<GEAR[2:0]> (clock gear). Although a setup can be changed during operation, after register writing before a clock actually changes, a maximum of 16-clock time is required of fc.

Page 19: The Setting Method Of A System Clock

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.6.1. The setting method of a system clock setup (internal oscillation → external oscillation) (1) f As a f setup, the example of switching procedure to the external oscillation (EHOSC) from an internal oscillation (IHOSC1) is shown below.

Page 20

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode setup (an external oscillation/external clock input → an internal oscillation) (3) f As a f setup, the example of switching procedure to the internal oscillation (IHOSC1) from an external oscillation (EHOSC) or an external clock input (EHCLKIN) is shown below. <<...

Page 21: Clock Supply Setting Function

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.2.7. Clock supply setting function This MCU has the clock on/off function for the peripheral circuits. To reduce the power consumption, this CPU can stop supplying the clock to the peripheral functions that are not used. Except some peripheral functions, clocks are not supplied after reset.

Page 22: Operation Mode

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3. Operation mode There are NORMAL mode and a Low Power Consumption mode (IDLE, STOP1, STOP2) in this product as an Operation mode, and it can reduce power consumption by performing mode changes according to directions for use.

Page 23: Low Power Consumption Mode

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode The product will be cut off the power except for the following circuit in STOP2 mode. ● External low speed oscillator (ELOSC) ● ● Backup RAM ● Port pin status ● ●...

Page 24

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode Table 1.7 Block operation status in each Low Power Consumption mode STOP1 STOP2 (Note1) Block NORMAL IDLE ELOSC ELOSC ELOSC ELOSC □ Processor core (Debug included) × × □ □ DMAC ×...

Page 25

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode Note3: The address match wake up function can only be used. Note4: A port state when the [RLMSHTDNOP] <PTKEEP> is set to "1" is held. Note5: It becomes a data hold when peripheral functions (DMA etc.) which carry out data access (R/W), except CPU, are not connected on the bus matrix.

Page 26: Mode State Transition

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.2. Mode State Transition Reset Reset After reset, (The backup domain) the high-speed oscillator1(IHOSC1) Interrupt (Note2) oscillates. Note2 STOP2 Mode Interrupt STOP1 Mode (CPU stops with shutdown NORMAL Mode (CPU stops except internal power supply some peripheral except some peripheral...

Page 27: Stop1 Mode Transition Flow

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.2.2. STOP1 mode transition flow Set up the following procedure at switching to STOP1. Because STOP1 mode is released by an interrupt, set the interrupt before switching to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "1.3.3.1.

Page 28: Stop2 Mode Transition Flow

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.2.3. STOP2 mode transition flow Set up the following procedure at switching to STOP2. Because STOP2 mode is released by an interrupt, set the interrupt before switching to STOP2 mode. For the interrupts that can be used to release the STOP2 mode, refer to "1.3.3.1.

Page 29: The Return Operation From A Low Power Consumption Mode

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.3. The return operation from a Low Power Consumption mode 1.3.3.1. The release source of a Low Power Consumption mode Interrupt, Non-Maskable Interrupt, and reset can perform release from a Low Power Consumption mode. The standby release source which can be used is decided by a Low Power Consumption mode.

Page 30

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode ● Released by an interrupt request When interrupt releases a Low Power Consumption mode, it is necessary to prepare so that interrupt may be detected by CPU. The interrupt used for release STOP1 or STOP2 mode needs to set for detecting the interrupt by INTIF other than a setting of CPU.

Page 31: Warming Up At The Release Of Low Power Consumption Mode

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.3.2. Warming up at the release of Low Power Consumption mode Warming up may be required because of stability of an internal oscillator at the time of mode transition. When shifting from STOP1 mode to a NORMAL mode, an internal oscillation is chosen automatically and the warming up timer is started.

Page 32: The Restart Operation From The Stop2 Mode

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.3.3. The restart operation from the STOP2 mode The restart operation flow from STOP2 mode release factor interrupt generating is as follows. Generate release factor Check reset flag (Note1) □ [RLMRSTFLGx] = xx

(it is checked by which factor reset has occured.) STOP2 release interrupt RESET_N pin or LVD reset...

Page 33: Clock Operation By Mode Transition

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.4. Clock operation by mode transition The clock operation at mode transition is shown below. 1.3.4.1. NORMAL → IDLE → NORMAL Operation mode transition CPU stops at IDLE mode. The clock supply to a peripheral function holds a setting state. Please perform operation/ stop by the register of each peripheral function, a clock supply setting function, etc.

Page 34: Normal → Stop2 → Reset → Normal Operation Mode Transition

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.3.4.3. NORMAL → STOP2 → RESET → NORMAL Operation mode transition Warming up is not performed when returning to NORMAL mode by reset. Even when returning to NORMAL mode except for RESET, it branches to the interrupt routine of reset. A reset operation is performed to an internal Main power domain after STOP2 mode released.

Page 35: Explanation Of Register

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4. Explanation of register 1.4.1. Register list The register related to CG and its address information is shown below. channel/unit Base address Peripheral Function Clock Control and Operation Mode 0x400F3000 A low speed oscillation/power 0x4003E400 control 1.4.1.1.

Page 36: Register Description

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2. Register description 1.4.2.1. [CGPROTECT] (CG write protection register) After Bit Symbol Type Function reset 31:8 Read as "0" Control write protection for the CG register (all registers except this register) PROTECT[7:0] 0xC1 0xC1: CG Registers are write enabled.

Page 37: Cgsyscr] (System Clock Control Register)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.3. [CGSYSCR] (System clock control register) After Bit Symbol Type Function reset 31:28 Read as "0" Indicates a prescaler clock (ΦT0) selection. 0000: fc 0100: fc / 16 1000: fc / 256 0001: fc / 2 0101: fc / 32 1001: fc / 512...

Page 38: Cgstbycr] (Standby Control Register)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.4. [CGSTBYCR] (Standby control register) After Bit Symbol Type Function reset 31:2 Read as "0" Selects a Low Power Consumption mode. 00: IDLE STBY[1:0] 01: STOP1 10: STOP2 11: Reserved 1.4.2.5. [CGSCOCR] (SCOUT Output control register) After Bit Symbol Type...

Page 39: Cgpll0Sel] (Pll Selection Register For Fsys)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.6. [CGPLL0SEL] (PLL selection register for fsys) After Bit Symbol Type Function reset PLL multiplication setup 31:8 PLL0SET[23:0] 0x000000 About a multiplication setup, refer to "1.2.5.2. The formula and the example of a setting of a PLL multiplication value". Read as "0"...

Page 40: Cgwuplcr] (Low Speed Oscillation Warming Up Register)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.8. [CGWUPLCR] (Low speed oscillation warming up register) After Bit Symbol Type Function reset 31:27 Read as "0" Sets the upper 15 bits of 19 bits of calculation values of the warm up timer.

Page 41: Cgfsysmenb] (Clock Supply And Stop Register B For Fsysm)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.9. [CGFSYSMENB] (Clock supply and stop register B for fsysm) After Bit Symbol Type Function reset IPMENB31 Read as "0". IPMENB30 Read as "0". IPMENB29 Read as "0". IPMENB28 Read as "0". IPMENB27 Read as "0".

Page 42: Cgfsysena] (Clock Supply And Stop Register A For Fsys)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.10. [CGFSYSENA] (Clock supply and stop register A for fsys) After Bit Symbol Type Function reset Enable the Clock

of T32A channel7 IPENA31 0: Clock stop 1: Clock supply Enable the Clock of T32A channel6 IPENA30 0: Clock stop 1: Clock supply...

Page 43 TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode After Bit Symbol Type Function reset Enable the Clock of PORT M IPENA11 0: Clock stop 1: Clock supply Enable the Clock of PORT L IPENA10 0: Clock stop 1: Clock supply Enable the Clock of PORT K IPENA09 0: Clock stop...

Page 44: Cgfsysenb] (Clock Supply And Stop Register B For Fsys)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.11. [CGFSYSENB] (Clock supply and stop register B for fsys) After Bit Symbol Type Function reset Clock enabling of SIWDT IPENB31 0: Clock stop 1: Clock supply IPENB30 Write as "1" IPENB29 Write as "1"...

Page 45 TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode After Bit Symbol Type Function reset 0: Clock stop 1: Clock supply Enable the Clock of UART channel3 IPENB08 0: Clock stop 1: Clock supply Enable the Clock of UART channel2 IPENB07 0: Clock stop 1: Clock supply...

Page 46: Cgfcen] (Clock Supply And Stop Register For Fc)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.12. [CGFCEN] (Clock supply and stop register for fc) After Bit Symbol Type Function reset 31:8 Read as "0" Enable the clock for DNF unit A, unit B and unit C. FCIPEN07 0: Clock stop 1: Clock supply...

Page 47: Rlmprotect] (Rlm Write Protection Register)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.4.2.16. [RLMPROTECT] (RLM write protection register) After Bit Symbol Type Function reset RLM register write protection control 0xC1: RLM registers are write enable Other than 0xC1: set write protection (protection enable) PROTECT 0xC1 If the write protection is set, you will not be able to write...

Page 48: Information According To Product

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.5. Information according to product The information about [CGFSYSMENB], [CGFSYSENA] and [CGFSYSENB] which are different according to each product is shown below. 1.5.1. [CGFSYSMENB] Table 1.10 Allocation of [CGFSYSMENB] by product Channel number/ Connection Bit Symbol...

Page 49: Cgfsysena]

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.5.2. [CGFSYSENA] Table 1.11 Allocation of [CGFSYSENA] by product Channel number/ Connection Bit Symbol Unit name/ I/O M3HQ M3HP M3HN M3HM M3HL destination port name □ □ □ □ □ IPENA31 T32A □...

Page 50: Cgfsysenb]

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 1.5.3. [CGFSYSENB] Table 1.12 Allocation of [CGFSYSENB] by product Channel number/ Connection Bit Symbol Unit name/ I/O M3HQ M3HP M3HN M3HM M3HL destination port name □ □ □ □ □ IPENB31 SIWDT IPENB30 ×...

Page 51: Memory Map

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2. Memory Map 2.1. Overview The memory maps for TMPM3H group (1) are based on the Arm Cortex-M3 processor core memory map. The internal ROM, internal RAM and special function registers (SFR) of TMPM3H group (1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M3 respectively.

Page 52: Tmpm3Hxfda

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2.1.1. TMPM3HxFDA ● Code Flash: 512KB ● RAM: 64KB ● Data Flash: 32KB ● Target products: TMPM3HQFDAFG, TMPM3HPFDAFG, TMPM3HPFDADFG, TMPM3HNFDAFG, TMPM3HNFDADFG, TMPM3HMFDAFG, TMPM3HLFDAUG 0xFFFFFFFF 0xFFFFFFFF Vendor-Specific Vendor-Specific 0xE0100000 0xE0100000 CPU Register Region CPU Register Region 0xE0000000 0xE0000000...

Page 53: Tmpm3Hxfza

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2.1.2. TMPM3HxFZA ● Code Flash: 384KB ● RAM: 64KB ● Data Flash: 32KB ● Target products: TMPM3HQFZAFG, TMPM3HPFZAFG, TMPM3HPFZADFG, TMPM3HNFZAFG, TMPM3HNFZADFG, TMPM3HMFZAFG, TMPM3HLFZAUG 0xFFFFFFFF 0xFFFFFFFF Vendor-Specific Vendor-Specific 0xE0100000 0xE0100000 CPU Register Region CPU Register Region 0xE0000000 0xE0000000...

Page 54: Tmpm3Hxfya

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2.1.3. TMPM3HxFYA ● Code Flash: 256KB ● RAM: 64KB ● Data Flash: 32KB ● Target products: TMPM3HQFYAFG, TMPM3HPFYAFG, TMPM3HPFYADFG, TMPM3HNFYAFG, TMPM3HNFYADFG, TMPM3HMFYAFG, TMPM3HLFYAUG 0xFFFFFFFF 0xFFFFFFFF Vendor-Specific Vendor-Specific 0xE0100000 0xE0100000 CPU Register Region CPU Register Region 0xE0000000 0xE0000000...

Page 55: Bus Matrix

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2.2. Bus Matrix This MCU contains two bus masters such as a CPU core and DMA controllers. Bus masters connect to slave ports (S0 to S4) of Bus Matrix. In the bus matrix, master ports (M0 to M14) connect to peripheral functions via connections described as (o) or (●) in the following figure.

Page 56: Single Boot Mode

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2.2.1.2. Single boot mode DMAC Cortex-M3 (unitB) System DMAC (unitA) Data Instruction Code Flash Data Flash GPREG RAM0 RAM1 IA (INTIF) RAM2 I2CS Backup RAM BOOT ROM TSPI (ch0/1) I2C, EI2C (ch0) UART (ch0/1/2/3) COMP T32A (ch0/1/2/3)

Page 57: Connection Table

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2.2.2. Connection table 2.2.2.1. Code area/ SRAM area (1) Single chip mode Table 2.1 Single chip mode Master DMAC DMAC Core Core Core Start Address Slave (Unit A) (Unit B) S-Bus D-Bus I-Bus □...

Page 58: Peripheral Area

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 2.2.2.2. Peripheral area Table 2.3 Peripheral area Master DMAC DMAC Core Core Core Start Address Slave (Unit A) (Unit B) S-Bus D-Bus I-Bus 0x40000000 Fault Fault Fault Fault □ 0x4003E000 IA (INTIF) Fault Fault □...

Page 59: Power Supply And Reset Operation

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3. Power Supply and Reset Operation 3.1. Outline This section describes how to turn on a power supply, and how to assert and deassert a Power On Reset and reset. Function classification Factor Functional Description Reset which occurs at the time of turning on or off a...

Page 60: Function And Operation

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2. Function and Operation This chapter explains about power on, power off, and reset. Note: Refer to the datasheet "Electrical Characteristics" chapter for the time and voltage of description of the symbol in a figure.

Page 61: Reset By A Power On Reset Circuit (Without Using A Reset_N Pin)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.1.1. Reset by a Power On Reset Circuit (without using a RESET_N pin) After a supply voltage exceeds the release voltage of a Power On Reset (POR), internal reset is deasserted after "Internal initialization time"...

Page 62: Reset By A Reset_N Pin

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.1.2. Reset by a RESET_N pin When turn on a power supply, it can control the timing of reset release by using RESET_N pin. After a supply voltage exceeds the release voltage of a Power On Reset and even after "Internal initialization time" elapsed and RESET_N pin is still "Low", internal reset is extended.

Page 63: Figure 3.3 Reset Operation By A Reset_N Pin (2)

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode In case of RESET_N pin input change from "Low" to "High" before "Internal initialization time" elapses, internal reset signal is released after "Internal initialization time" elapses. Please goes up a supply voltage into an operating voltage range before "Internal initialization time" elapses. The CPU operates after internal reset release.

Page 64: Continuation Of Reset By Lvd

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.1.3. Continuation of reset by LVD When the power supply voltage has not exceeded the LVD release voltage even after "Internal initialization time" elapses, LVD generates the reset signal and the reset state continues. After the power supply voltage exceeds the LVD release voltage and "LVD detection release time"...

Page 65: Warm Reset

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.2. Warm reset 3.2.2.1. Warm reset by RESET_N pin When resetting with the RESET_N pin, set the RESET_N pin to "Low" for at least 17.2 µs or more while the power supply voltage is within the operating range. When the "Low"...

Page 66: Reset By Stop2 Mode Release

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.3. Reset by STOP2 mode release When RESET_N pin is changed to "Low" or LVD reset occurred during STOP2 mode, STOP2 released. The power supply is turned on and assert reset to Main Power Domain. After RESET_N pin is changed to "High" or LVD reset is released, start operation in NORMAL mode.

Page 67: Figure 3.7 Starting In The Single Boot Mode When Power Supply Is Stable

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode When the supply voltage is stable within an operating voltage range, input "Low" to RESET_N pin for reset equal to or longer than "Internal processing time", while "Low" is input to the BOOT_N pin. DVDD5 = DVDD5A = DVDD5B = AVDD5 DVDD5 Operation Voltage range...

Page 68: Power On Reset Circuit

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.5. Power On Reset Circuit The Power On Reset Circuit (POR) generates a reset signal when the power is turned on or turned off. Note: The Power On Reset Circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electrical characteristics.

Page 69: Turning Off And Re-Turning On Power Supply

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.6. Turning off and re-turning on power supply When a power supply is turned off, a power supply voltage must be down gentler gradient than Max value of “Power gradient (V)”...

Page 70: A Reset Factor And The Reset Initialized Range

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 3.2.7.1. A reset factor and the reset initialized range A reset factor and the range initialized are shown in Table 3.1. Table 3.1 A reset factor and the initialized range Reset factors STOP2 mode Cold Warm reset (Note1)

Page 71: Revision History

TXZ+ Family TMPM3H Group(1) Clock Control and Operation Mode 4. Revision History Table 4.1 Revision History Revision Date Description 2021-05-21 First release - Corrected Figure 1.3. - 1.3.3.1. The release source of a Low Power Consumption mode Changed description. - 1.3.3.3. The restart operation from the STOP2 mode Changed Note2 to Note3, and Note3 is corrected.

Page 72: Restrictions On Product Use

Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the

specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook"...

This manual is also suitable for:

Tmpm3hCg-m3h-dCg-m3h1-d