



Asus AAEON COM-BT-A30 User Manual

Com express module

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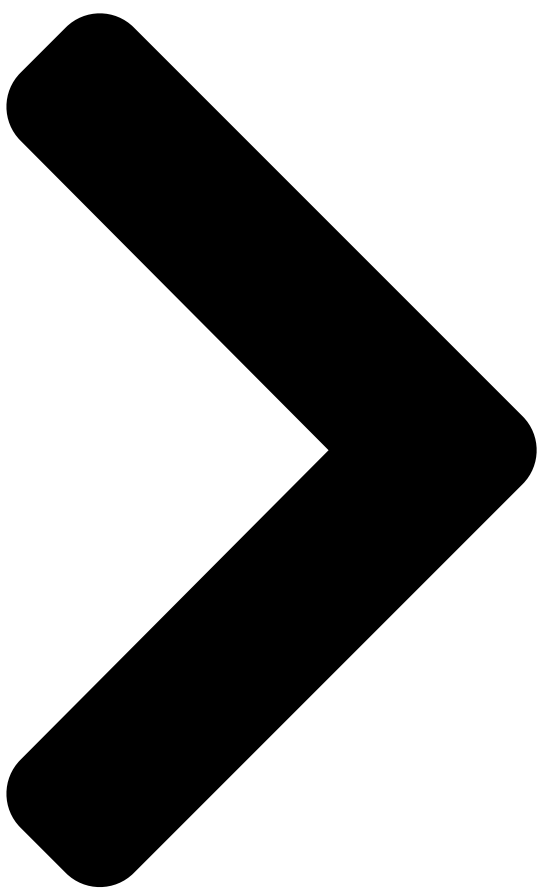
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Summary of Contents for Asus AAEON COM-BT-A30

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respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. Intel, Pentium, Celeron, and Xeon are registered trademarks of Intel Corporation Core, Atom are trademarks of Intel Corporation

[Page 4](#) Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity COM-BT-A30 If any of these items are missing or damaged, please contact your distributor or sales representative immediately. Preface...

[Page 5](#) About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the AAEON.com for the latest version of this document.

[Page 6](#) Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

[Page 7](#) If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

[Page 8](#) FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

[Page 9](#) China RoHS Requirements (CN) AAEON Main Board/ Daughter Board/ Backplane (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) ...

[Page 10](#) China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Main Board/ Daughter Board/ Backplane Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) PCB &...

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Chapter 1 Chapter 1 - Product Specifications...

[Page 14: Specifications](#)

Specifications System COM Express, Compact, Pin-out Type 6 Form Factor Onboard Intel® Atom™ SoC Intel® Atom™ N2930 (1.83 GHz) CPU Frequency N2807 (1.58 GHz) E3845 (1.91 GHz) E3827 (1.75 GHz) E3825 (1.33 GHz) J1900 (2.0 GHz) Intel® Atom™ SoC Chipset DDR3L 1066/1333 MHz SODIMM x 1 Memory Type 8 GB Max.

[Page 15](#) System -40°F ~ 176°F (-40°C ~ 80°C) Storage Temperature 0% ~ 90% relative humidity, non-condensing Operating Humidity 80,000 MTBF (Hours) CE/FCC Certification Display VGA/LCD Controller Intel® Atom™ SoC Integrated Video Output CRT, LVDS LCD, DDI Intel® I211, Gigabit Ethernet Ethernet High Definition Audio Interface Audio USB 2.0 x 7, USB 3.0 x 1...

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Chapter 2 Chapter 2 – Hardware Information...

[Page 17: Dimensions](#)

Dimensions Component Side Chapter 2 – Hardware Information...

[Page 18 Solder Side With Heat spreader Chapter 2 – Hardware Information...](#)

[Page 19: Jumpers And Connectors](#)

Jumpers and Connectors Component Side Chapter 2 – Hardware Information...

[Page 20 Solder Side Chapter 2 – Hardware Information...](#)

[Page 21: List Of Connectors](#)

List of Connectors Please refer to the table below for all of the board's jumpers that you can configure for your application Label Function 1. Carrier Board DP/HDMI Function 2. LVDS Function 3. AT & ATX mode 4. RCT Rest setting BAT1 RTC Battery ROW A/B...

[Page 22: Rct Rest Setting \(Sw1\)](#)

2.3.1 Carrier Board DP/HDMI Function, LVDS Function, AT & ATX Mode, RCT Rest Setting (SW1) DP/HDMI[1](Default) eDP on MB(Optional) DP/HDMI[2](Optional) LVDS(Default) ATX (Default) Normal(Default) Clear CMOS 2.3.2 COM Express ROW A/B Connector (CN1) Row A COMe 2.1 SPEC Type 6 COM-BT Signal GBE0_MDI3- GBE0_MDI3-...

[Page 23](#) SUS_S3# SUS_S3# SATA0_TX+ SATA0_TX+ SATA0_TX- SATA0_TX- SUS_S4# SUS_S4# SATA0_RX+ SATA0_RX+ SATA0_RX- SATA0_RX- SATA2_TX+ SATA2_TX- SUS_S5# SUS_S5# SATA2_RX+ SATA2_RX- BATLOW# BATLOW# (S)ATA_ACT# (S)ATA_ACT# AC/HDA_SYNC AC/HDA_SYNC AC/HDA_RST# AC/HDA_RST# AC/HDA_BITCLK AC/HDA_BITCLK AC/HDA_SDOUT AC/HDA_SDOUT BIOS_DIS0# BIOS_DIS0# THRMTRIP# THRMTRIP# USB6- USB6- USB6+ USB6+ USB_6_7_OC# USB_6_7_OC# USB4- USB4- USB4+...

[Page 24](#) USB2- USB2- USB2+ USB2+ USB_2_3_OC# USB_2_3_OC# USB0- USB0- USB0+ USB0+ VCC_RTC VCC_RTC EXCD0_PERST# EXCD0_PERST# EXCD0_CPPE# EXCD0_CPPE# LPC_SERIRQ LPC_SERIRQ PCIE_TX5+ PCIE_TX5- GPIO GPIO PCIE_TX4+ PCIE_TX4- PCIE_TX3+ PCIE_TX3- PCIE_TX3- PCIE_TX2+ PCIE_TX2+ PCIE_TX2- PCIE_TX2- GPI1 GPI1 PCIE_TX1+ PCIE_TX1+ PCIE_TX1- PCIE_TX1- GPI2 GPI2 PCIE_TX0+ PCIE_TX0+ Chapter 2 -...

[Page 25](#) PCIE_TX0- PCIE_TX0- LVDS_A0+ LVDS_A0+ LVDS_A0- LVDS_A0- LVDS_A1+ LVDS_A1+ LVDS_A1- LVDS_A1- LVDS_A2+ LVDS_A2+ LVDS_A2- LVDS_A2- LVDS_VDD_EN LVDS_VDD_EN LVDS_A3+ LVDS_A3+ LVDS_A3- LVDS_A3- LVDS_A_CK+ LVDS_A_CK+ LVDS_A_CK- LVDS_A_CK- LVDS_I2C_CK LVDS_I2C_CK LVDS_I2C_DAT LVDS_I2C_DAT GPI3 GPI3 RSVD_RSVD PCIE_CLK_REF+ PCIE_CLK_REF+ PCIE_CLK_REF- PCIE_CLK_REF- SPI_POWER SPI_POWER SPI_MISO SPI_MISO GPO0 GPO0 SPI_CLK...

[Page 26](#) TPM_PP TPM_PP TYPE10# SER0_TX SER0_TX SER0_RX SER0_RX A100 A101 SER1_TX SER1_TX A102 SER1_RX SER1_RX A103 LID# LID# A104 VCC_12V VCC_12V A105 VCC_12V VCC_12V A106 VCC_12V VCC_12V A107 VCC_12V VCC_12V A108 VCC_12V VCC_12V A109 VCC_12V VCC_12V A110 Row B COMe 2.1 SPEC Type 6 COM-BT Signal GBE0_ACT# GBE0_ACT#...

[Page 27](#) LPC_CLK LPC_CLK PWRBTN# PWRBTN# SMB_CK SMB_CK SMB_DAT SMB_DAT SMB_ALERT# SMB_ALERT# SATA1_TX+ SATA1_TX+ SATA1_TX- SATA1_TX- SUS_STAT# SUS_STAT# SATA1_RX+ SATA1_RX+ SATA1_RX- SATA1_RX- SATA3_TX+ SATA3_TX- PWR_OK PWR_OK SATA3_RX+ SATA3_RX- AC/HDA_SDIN2 AC/HDA_SDIN2 AC/HDA_SDIN1 AC/HDA_SDIN1 AC/HDA_SDIN0 AC/HDA_SDIN0 SPKR SPKR I2C_CK I2C_CK I2C_DAT I2C_DAT THRM# THRM# USB7- Chapter 2 -...

[Page 28](#) USB7+ USB_4_5_OC# USB_4_5_OC# USB5- USB5- USB5+ USB5+ USB3- USB3- USB3+ USB3+ USB_0_1_OC# USB_0_1_OC# USB1- USB1- USB1+ USB1+ EXCD1_PERST# EXCD1_PERST# EXCD1_CPPE# EXCD1_CPPE# SYS_RESET# SYS_RESET# CB_RESET# CB_RESET# PCIE_RX5+ PCIE_RX5- GPO1 GPO1 PCIE_RX4+ PCIE_RX4- GPO2 GPO2 PCIE_RX3+

PCIE_RX3+ PCIE_RX3- PCIE_RX3- PCIE_RX2+ PCIE_RX2+ PCIE_RX2- PCIE_RX2- GPO3 GPO3...

[Page 29](#) PCIE_RX1+ PCIE_RX1+ PCIE_RX1- PCIE_RX1- WAKE0# WAKE0# WAKE1# WAKE1#
PCIE_RX0+ PCIE_RX0+ PCIE_RX0- PCIE_RX0- LVDS_B0+ LVDS_B0+ LVDS_B0- LVDS_B0-
LVDS_B1+ LVDS_B1+ LVDS_B1- LVDS_B1- LVDS_B2+ LVDS_B2+ LVDS_B2- LVDS_B2- LVDS_B3+
LVDS_B3+ LVDS_B3- LVDS_B3- LVDS_BKLT_EN LVDS_BKLT_EN LVDS_B_CK+ LVDS_B_CK+
LVDS_B_CK- LVDS_B_CK- LVDS_BKLT_CTRL LVDS_BKLT_CTRL VCC_5V_SBY VCC_5V_SBY
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[Page 30](#) VGA_GRN VGA_GRN VGA_BLU VGA_BLU VGA_HSYNC VGA_HSYNC VGA_VSYNC
VGA_VSYNC VGA_I2C_CLK VGA_I2C_CLK VGA_I2C_DAT VGA_I2C_DAT SPI_CS# SPI_CS# RSVD SMI#
RSVD SCI# B100 B101 FAN_PWMOUT FAN_PWMOUT B102 FAN_TACHIN FAN_TACHIN B103
SLEEP# SLEEP# B104 VCC_12V VCC_12V B105 VCC_12V VCC_12V B106 VCC_12V VCC_12V
B107 VCC_12V VCC_12V B108 VCC_12V VCC_12V...

[Page 31: Com Express Row C/D Connector \(Cn2\)](#)

2.3.3 COM Express ROW C/D Connector (CN2) Row C COMe 2.1 SPEC Type 6 COM-BT Signal
USB_SSRX0- USB_SSRX0- USB_SSRX0+ USB_SSRX0+ USB_SSRX1- USB_SSRX1+ USB_SSRX2-
USB_SSRX2+ USB_SSRX3- USB_SSRX3+ DDI1_PAIR6+ DDI1_PAIR6- RSVD RSVD PCIE_RX6+
PCIE_RX6- PCIE_RX7+ PCIE_RX7- Chapter 2 - Hardware Information...

[Page 32](#) DDI1_HPD DDI1_HPD DDI1_PAIR4+ DDI1_PAIR4- RSVD RSVD DDI1_PAIR5+
DDI1_PAIR5- DDI2_CTRLCLK_AUX+ DDI2_CTRLCLK_AUX- DDI2_CTRLCLK_AUX-
DDI2_CTRLCLK_AUX- DDI2_DDC_AUX_SEL DDI2_DDC_AUX_SEL RSVD DDI3_CTRLCLK_AUX+
DDI3_CTRLCLK_AUX- DDI3_DDC_AUX_SEL DDI3_PAIR0+ DDI3_PAIR0- DDI3_PAIR1+
DDI3_PAIR1- DDI3_HPD RSVD DDI3_PAIR2+ DDI3_PAIR2- RSVD DDI3_PAIR3+ DDI3_PAIR3-
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[Page 33](#) PEG_RX0+ PEG_RX0- TYPE0# PEG_RX1+ PEG_RX1- TYPE1# PEG_RX2+ PEG_RX2-
PEG_RX3+ PEG_RX3- RSVD RSVD PEG_RX4+ PEG_RX4- RSVD PEG_RX5+ PEG_RX5- PEG_RX6+
PEG_RX6- PEG_RX7+ PEG_RX7- RSVD Chapter 2 - Hardware Information...

[Page 34](#) PEG_RX8+ PEG_RX8- PEG_RX9+ PEG_RX9- RSVD PEG_RX10+ PEG_RX10-
PEG_RX11+ PEG_RX11- PEG_RX12+ PEG_RX12- PEG_RX13+ PEG_RX13- RSVD PEG_RX14+
PEG_RX14- C100 C101 PEG_RX15+ C102 PEG_RX15- C103 C104 VCC_12V VCC_12V Chapter 2 -
Hardware Information...

[Page 35](#) C105 VCC_12V VCC_12V C106 VCC_12V VCC_12V C107 VCC_12V VCC_12V C108
VCC_12V VCC_12V C109 VCC_12V VCC_12V C110 Row D COMe 2.1 SPEC Type 6 COM-BT Signal
USB_SSTX0- USB_SSTX0- USB_SSTX0+ USB_SSTX0+ USB_SSTX1- USB_SSTX1+ USB_SSTX2-
USB_SSTX2+ USB_SSTX3- USB_SSTX3+ DDI1_CTRLCLK_AUX+ DDI1_CTRLCLK_AUX+
DDI1_CTRLCLK_AUX- DDI1_CTRLCLK_AUX- RSVD RSVD Chapter 2 -...

[Page 36](#) PCIE_TX6+ PCIE_TX6- PCIE_TX7+ PCIE_TX7- RSVD RSVD DDI1_PAIR0+ DDI1_PAIR0+
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DDI1_PAIR2+ DDI1_PAIR2+ DDI1_PAIR2- DDI1_PAIR2- DDI1_DDC_AUX_SEL DDI1_DDC_AUX_SEL
RSVD DDI1_PAIR3+ DDI1_PAIR3+ DDI1_PAIR3- DDI1_PAIR3- RSVD DDI2_PAIR0+ DDI2_PAIR0+
DDI2_PAIR0- DDI2_PAIR0- DDI2_PAIR1+ DDI2_PAIR1+ DDI2_PAIR1- DDI2_PAIR1- DDI2_HPD
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[Page 37](#) DDI2_PAIR2+ DDI2_PAIR2+ DDI2_PAIR2- DDI2_PAIR2- RSVD DDI2_PAIR3+
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PEG_TX1- TYPE2# TYPE2# PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- RSVD RSVD PEG_TX4+
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D100 D101 PEG_TX15+ D102 PEG_TX15- D103 D104 VCC_12V VCC_12V D105 VCC_12V
VCC_12V D106 VCC_12V VCC_12V D107 VCC_12V VCC_12V D108 VCC_12V VCC_12V D109
VCC_12V VCC_12V D110 2.3.4 SPI Connector (CN5) Signal Signal SPI_S0_F SPI_S1_F SPI_CE0#_F

[Page 40: Lpc Connector \(Cn6\)](#)

2.3.5 LPC Connector (CN6) Signal Signal LPC_AD0 BUF_PLT_RST# LPC_AD1 LPC_AD2
PCI_CLK_SIO LPC_AD3 +V3.3S LPC_FRAME# INT_SERIRQ Chapter 2 – Hardware Information...

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Chapter 3 Chapter 3 - AMI BIOS Setup...

[Page 42: System Test And Initialization](#)

System Test and Initialization These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

[Page 43: Ami Bios Setup](#)

AMI BIOS Setup AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off. Entering Setup Power on the computer and press or <ESC>...

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Setup submenu: Main Chapter 3 – AMI BIOS Setup...

[Page 45: Setup Submenu: Advanced](#)

Setup submenu: Advanced Chapter 3 – AMI BIOS Setup...

[Page 46: Advanced: Cpu Configuration](#)

3.4.1 Advanced: CPU Configuration Options summary: Intel Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. EIST Disabled Enabled Optimal Default, Failsafe Default Enable/Disable Intel SpeedStep. Chapter 3 – AMI BIOS Setup...

[Page 47: Advanced: Ide Configuration](#)

3.4.2 Advanced: IDE Configuration Options summary: SATA Mode IDE Mode AHCI Mode Optimal Default, Failsafe Default Select IDE / AHCI. Chapter 3 – AMI BIOS Setup...

[Page 48: Advanced: Usb Configuration](#)

3.4.3 Advanced: USB Configuration Options summary: Legacy USB Support Enabled Optimal Default, Failsafe Default Disabled Auto Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications. Device Name (Emulation Auto Optimal Default, Failsafe Default...

[Page 49](#) If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive) Chapter 3 – AMI BIOS Setup...

[Page 50: Advanced: On-Module H/W Monitor](#)

3.4.4 Advanced: On-Module H/W Monitor Options summary: CPU Smart Fan Mode Configuration Chapter 3 – AMI BIOS Setup...

[Page 51: Cpu Smart Fan Control: Full Mode](#)

3.4.4.1 CPU Smart Fan control: Full mode Chapter 3 – AMI BIOS Setup...

[Page 52: Cpu Smart Fan Control: Manual Mode By Pwm](#)

3.4.4.2 CPU Smart Fan control: Manual Mode by PWM Options summary: Manual Setting Optimal Default, Failsafe Default Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number.

[Page 53: Cpu Smart Fan Control: Auto Mode By Pwm](#)

3.4.4.3 CPU Smart Fan control: Auto Mode by PWM Options summary: Temperature of Optimal Default, Failsafe Default Start Temperature of Start Temperature of Off 20 Optimal Default, Failsafe Default Temperature of Off Start PWM Optimal Default, Failsafe Default Start PWM Slope (PWM) 0 (PWM) 1 (PWM)

[Page 54](#) 8 (PWM) 16 (PWM) 32 (PWM) 64 (PWM) Slope (PWM) Chapter 3 – AMI BIOS Setup...

[Page 55: Advanced: Dynamic Digital Io Configuration](#)

3.4.5 Advanced: Dynamic Digital IO Configuration Options summary: GPI* Direction Output Input Optimal Default, Failsafe Default Set GPIO as Input or Output GPO* Direction Output Optimal Default, Failsafe Default Input Set GPIO as Input or Output Output Level Optimal Default, Failsafe Default Set GPIO Output as Hi or Low.

[Page 56: Advanced: Power Management](#)

3.4.6 Advanced: Power Management Options summary: Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select power supply mode. Restore on Power Last State Optimal Default, Failsafe Default Loss Always On Always Off Power failure feature / AC Power Loss feature. RTC wake system Disabled Optimal Default, Failsafe Default...

[Page 57](#) Fixed Time : System will wake on the hr::min::sec specified. Dynamic Time : System will wake on the current time + Increase minute(s). Chapter 3 – AMI BIOS Setup...

[Page 58: Advanced: Trusted Computing](#)

3.4.7 Advanced: Trusted Computing Options summary: Security Device Disable Optimal Default, Failsafe Default Support Enable Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. Chapter 3 – AMI BIOS Setup...

[Page 59](#) Options summary: Security Device Disable Optimal Default, Failsafe Default Support Enable Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. Pending operation None Optimal Default, Failsafe Default TPM Clear Schedule an Operation for the Security Device.

[Page 60](#) Enable Optimal Default, Failsafe Default Storage Hierarchy HELP . Endorsement Disable Hierarchy Enable Optimal Default, Failsafe Default Endorsement Hierarchy HELP . Chapter 3 – AMI BIOS Setup...

[Page 61: Advanced: Sio Configuration](#)

3.4.8 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

[Page 62: Serial Port 9 Configuration](#)

3.4.8.1 Serial Port 9 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default Enable or Disable this logical device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2D8h; IRQ=11; DMA; IO=2C8h; IRQ=11; DMA; Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.

[Page 63: Serial Port 10 Configuration](#)

3.4.8.2 Serial Port 10 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default Enable or Disable this logical device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2C8h; IRQ=10; DMA; IO=2D8h; IRQ=10; DMA; Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.

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Setup submenu: Chipset Chapter 3 – AMI BIOS Setup...

[Page 65: Chipset: North Bridge](#)

3.5.1 Chipset: North Bridge Chapter 3 – AMI BIOS Setup...

[Page 66: North Bridge: Display Control Configuration](#)

3.5.1.1 North Bridge: Display Control Configuration Options summary: DVMT Pre-Allocated Optimal Default, Failsafe Default 128M 160M ... 512M Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device. DVMT Total Gfx Mem 128MB 256MB Optimal Default, Failsafe Default Select DVMT 5.0 Total Graphics Memory size used by the Internal Graphics Device.

[Page 67](#) Primary IGFX Boot VBIOS Default Optimal Default, Failsafe Default Display LVDS DP/HDMI Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display LVDS Panel Type 640x480, 60Hz 800x480, 60Hz...

[Page 68](#) Panel Mode Single Channel Dual Channel Optimal Default, Failsafe Default Single Channel / Dual Channel. Data enable polarity Active Low Optimal Default, Failsafe Default Active High Active High / Low . LVDS Backlight Level 100% Optimal Default, Failsafe Default Select Backlight brightness of LVDS. LVDS Backlight Type Normal Optimal Default, Failsafe Default...

[Page 69: Chipset: South Bridge](#)

3.5.2 Chipset: South Bridge Options summary: xHCI Mode Enabled Optimal Default, Failsafe Default Disabled Mode of operation of xHCI controller. Audio Controller Enabled Optimal Default, Failsafe Default Disabled Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally Enabled.

[Page 70: Setup Submenu: Security](#)

Setup submenu: Security Change User/ Supervisor Password You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility. If you highlight these items and press Enter, a dialog box appears which lets you enter a password.

[Page 71: Setup Submenu: Boot](#)

Setup submenu: Boot Options summary: Quiet Boot Disabled Enabled Default Enables or Disables Quiet Boot option. Option ROM Messages Force BIOS Default Keep Current Set display mode for Option ROM Launch PXE OpROM Disabled Default Enabled Controls the execution of LAN PXE OpROM. Chapter 3 –...

[Page 72: Bbs Priorities](#)

3.7.1 BBS Priorities Chapter 3 – AMI BIOS Setup...

[Page 73: Setup Submenu: Save & Exit](#)

Setup submenu: Save & Exit Chapter 3 – AMI BIOS Setup...

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Chapter 4 Chapter 4 – Drivers Installation...

[Page 75: Driver Download/Installation](#)

Driver Download/Installation Drivers for the COM-BT-A30 can be downloaded from the product page on the AAEON website by following this link: <https://www.aaeon.com/en/p/modulescom-express-modules-com-bt> Download the driver(s) you need and follow the steps below to install them. Step 1 – Install Chipset Driver Open the Step1 - Chipset folder followed by SetupChipset.exe Follow the instructions Drivers will be installed automatically...

[Page 76](#) Step 4 – Install xHCI Driver Open the STEP4 - xHCI folder Open the Setup.exe file in the folder Follow the instructions Drivers will be installed automatically Step 5 – Install Intel Sideband Fabric Device Driver Open the Step5 – Intel Sideband Fabric Device folder Open the

Setup.exe file in the folder Follow the instructions Drivers will be installed automatically...

[Page 77: Appendix A - Watchdog Timer Programming](#)

Appendix A Appendix A - Watchdog Timer Programming...

[Page 78: Watchdog Timer Initial Program](#)

Watchdog Timer Initial Program Table 1 : Embedded BRAM relative register table Default Value
Note Index 0x284(Note1) BRAM Index Register Data 0x285(Note2) BRAM Data Register Logical
Device Number 0xA8(Note3) Watch dog Logical Device Number Function and Device Number
0x00(Note4) Watch dog Function/Device Number Table 2 : Watchdog relative register table
Option BitNum...

[Page 79](#) *****
// Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex
//This parameter is represented from Note1 #define byte EcBRAMData //This parameter is
represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3
#define byte BRAMFnDataReg //This parameter is represented from Note4 #define void
EcBRAMWriteByte(byte Offset, byte Value);...

[Page 80](#) *****
VOID Main(){ // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) //
(boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure :
AaeonWDTEnable // This procedure will enable the WDT counting. AaeonWDTEnable();
***** Appendix A
- Watchdog Timer Programming...

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// Procedure : AaeonWDTEnable VOID AaeonWDTEnable () { WDTEnableDisable(1); // Procedure :
AaeonWDTConfig VOID AaeonWDTConfig () { // Disable WDT counting WDTEnableDisable(0); //
WDT relative parameter setting WDTParameterSetting(); VOID WDTEnableDisable(byte Value){
ECBRAMWriteByte(TimerReg , Value); VOID WDTParameterSetting(){ Byte TempByte; //
Watchdog Timer counter setting ECBRAMWriteByte(TimerReg , TimerVal);...

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VOID ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){ IOWriteByte(EcBRAMIndex,
0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData,
0x30); //Write start Byte ECBRAMReadByte(byte OPReg){ IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x12);
IOWriteByte(EcBRAMData, 0x10);...

[Page 83: Appendix B -I/O Information](#)

Appendix B Appendix B -I/O Information...

[Page 84: I/O Address Map](#)

I/O Address Map Appendix B - I/O Information...

[Page 85: Memory Address Map](#)

Memory Address Map IRQ Mapping Chart Appendix B - I/O Information...

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[Page 90](#) Appendix B – I/O Information...

[Page 91](#) Appendix B – I/O Information...

[Page 92: Appendix C - Programming Digital I/O](#)

Appendix C Appendix C – Programming Digital I/O...

[Page 93: Dio Programming](#)

DIO Programming COM-BT-A30 utilizes AAEON chipset as its Digital I/O controller. Below are the procedures to complete its configuration which you can develop customized program to fit your application. Appendix C – Programming Digital I/O...

[Page 94: Digital I/O Register](#)

Digital I/O Register Table 1 : Embedded BRAM relative register table Default Value Note Index
0x284(Note1) BRAM Index Register Data 0x285(Note2) BRAM Data Register Logical Device
Number 0xA2(Note3) Watch dog Logical Device Number Input/Output DIO Input/Output
Function/Device Function and Device 0x00(Note4) Number Number...

[Page 95: Digital I/O Sample Program](#)

Digital I/O Sample Program

```
***** //  
Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex  
//This parameter is represented from Note1 #define byte EcBRAMData //This parameter is  
represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3  
#define byte BRAMFnData0Reg //This parameter is represented from Note4 #define byte  
BRAMFnData1Reg //This parameter is represented from Note5 #define void  
EcBRAMWriteByte(byte Offset, byte Value);...
```

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```
VOID Main(){ Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read  
Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin  
level is High PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit); // Procedure :  
AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...
```

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```
Boolean AaeonReadPinStatus(byte OptionReg, byte BitNum){ Byte TempByte; TempByte =  
ECBRAMReadByte(BRAMFnData1Reg, OptionReg); If (TempByte & BitNum == 0) Return 0;  
Return 1; VOID AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){ Byte  
TempByte; TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg); TempByte |= (Value  
<< BitNum); ECBRAMWriteByte(OptionReg, BitNum, Value);...
```

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```
VOID ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){ IOWriteByte(EcBRAMIndex,  
0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);  
IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg);  
IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData,  
0x30); //Write start Byte ECBRAMReadByte(byte FnDataReg, byte OPReg){  
IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg);  
IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, FnDataReg);  
IOWriteByte(EcBRAMIndex, 0x12);...
```