



Asus Aaeon FWS-2273E7-A10-A10-00 User Manual

Desktop network appliance

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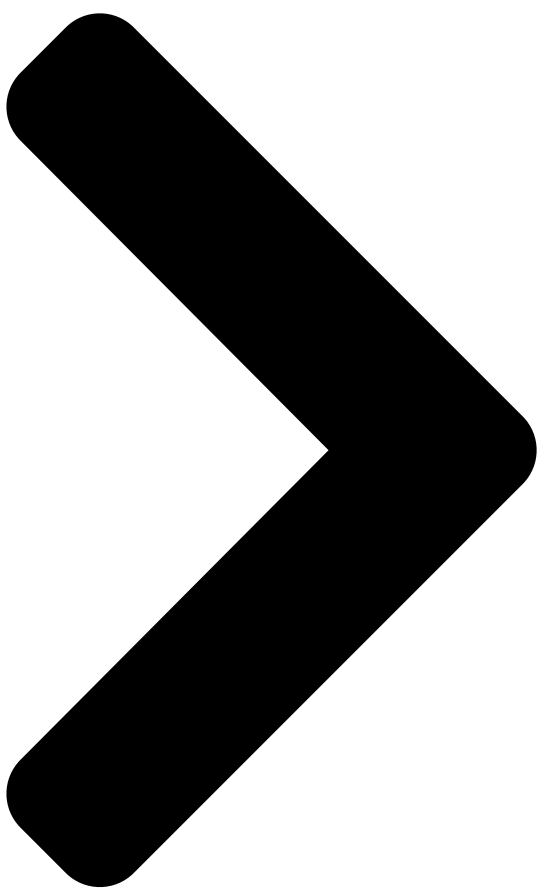
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Summary of Contents for Asus Aaeon FWS-2273E7-A10-A10-00

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[Page 2](#) Copyright Notice This document is copyrighted, 2019. All rights are reserved. The original manufacturer reserves the right to make improvements to the products described in this manual at any time without notice. No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means without the prior written permission of

the original manufacturer.

[Page 3](#) Acknowledgement All other products' name or trademarks are properties of their respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. Intel, Pentium, Celeron, and Xeon are registered trademarks of Intel Corporation Core, Atom are trademarks of Intel Corporation...

[Page 4](#) Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity FWS-2273 1 SATA cable 1 SATA power cable 1 Power adapter 1 Rubber foot 1 If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

[Page 5](#) About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the AAEON.com for the latest version of this document.

[Page 6](#) Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale.

[Page 7](#) As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers. If any of the following situations arises, please contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii.

[Page 8](#) FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation. Caution: There is a danger of explosion if the battery is incorrectly replaced.

[Page 9](#) China RoHS Requirements (CN) AAEON Embedded Box PC/ Industrial System (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) ...

[Page 10](#) China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Embedded Box PC/ Industrial System Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) PCB &...

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[Page 12](#) 3.4.6.1.2 Console Redirection Settings 50 3.4.7 Advanced: Power Management..... 57 3.4.8 Digital IO Port Configuration59 Setup submenu: Chipset 60 3.5.1 Chipset: North Bridge61 3.5.1.1 North Bridge: AMI Graphic Output Protocol Policy62 Setup submenu: Security 63 Setup submenu: Boot

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Chapter 1 Chapter 1 – Product Specifications...

[Page 14: Specifications](#)

Specifications System Desktop Network Appliance Form Factor Intel® Celeron® N3350 Processor SoC Processor Intel® Celeron® N3350 Processor SoC Chipset 204-pin DDR3L SODIMM x 1, up to 8GB System Memory Network Ethernet Intel® i211, Gigabit Ethernet x 4 Intel® i210,

SFP Bypass Supports up to 2 pairs bypass function Display...

[Page 15](#) Internal/ Expansion Interface PCIe Slot — Mini-PCIe Slot Mini-Card socket (full-size) with SIM socket x 2 KB Mouse Reserve pin-header USB 3.0 x 2 Miscellaneous Internal RTC Watchdog Timer 1~255 steps by software programmable (TPM v1.2 9660/TPM2.0 9665 Optional) GPIO Reserve internal pin header 8-bit Digital I/O interface (4-in /4-out) Fanless, reserved pin header for system fan...

[Page 16](#) Environmental Parameters and Dimension 12V DC Power in connector Power Requirement 32°F ~ 104°F (0°C ~ 40°C) Operating Temperature -4°F ~ 140°F (-20°C ~ 60°C) Storage Temperature 10%~80% relative humidity, non-condensing Operating Humidity 10%~80% @40°C; non-condensing Storage Humidity 0.5 Grms/ 5 ~ 500Hz / operation (2.5" HDD) Vibration 1.5 Grms/ 5 ~ 500Hz / non operation 10 G peak acceleration (11 m sec.

[Page 17: Chapter 2 - Hardware Information](#)

Chapter 2 Chapter 2 – Hardware Information...

[Page 18: Dimensions](#)

Dimensions System Chapter 2 – Hardware Information...

[Page 19](#) Board Component Side Solder Side Chapter 2 – Hardware Information...

[Page 20: Jumpers And Connectors](#)

Jumpers and Connectors Component Side Chapter 2 – Hardware Information...

[Page 21](#) Solder Side Chapter 2 – Hardware Information...

[Page 22: List Of Jumpers](#)

List of Jumpers Please refer to the table below for all of the board's jumpers that you can configure for your application Label Function CF POWER Selection Auto PWRBTN Selection CMOS Setting Selection Chapter 2 – Hardware Information...

[Page 23: Cfd Voltage 3.3V/5V Selection \(Jp1\)](#)

2.3.1 CFD Voltage 3.3V/5V Selection (JP1) 3.3V (Default) 2.3.2 Auto PWRBTN Selection (JP2) Don't use Auto PWRBTN (Default) Use Auto PWRBTN 2.3.3 CMOS Setting Selection (CN1) Normal (Default) Clear CMOS Chapter 2 – Hardware Information...

[Page 24: List Of Connectors](#)

List of Connectors Please refer to the table below for all of the board's connectors that you can configure for your application Label Function DIMM1 DDR3L SODIMM SOCKET CPU_FAN1 4P SMART FAN CON1 COM PORT CN12 SATA6G INTERFACE SATA POWER CN13 Mini PCIe socket (Only USB2.0) CN30...

[Page 25](#) LED4-LED7 RJ45 LAN Link Stats LED LED9-LED10 SFP LAN Link Stats LED Chapter 2 – Hardware Information...

[Page 26: Digital I/O \(Cn6\)](#)

2.4.1 Digital I/O (CN6) This connector offers 4-pair of digital I/O functions and address is 801H. The pin definitions are illustrated below: Signal Signal Digital- IN/OUT(Port1 Bit 1) Digital- IN/OUT (Port1 Bit 2) Digital- IN/OUT (Port1 Bit 4) Digital- IN/OUT (Port1 Bit 5) Digital- IN/OUT (Port3 Bit 4) Digital- IN/OUT (Port3 Bit 5) Digital- IN/OUT (Port6 Bit 3)

[Page 27: Hard Disk Drive Installation](#)

2.5" Hard Disk Drive Installation Loosen the screw and remove the top case from the lower side. Loosen the screw and remove the mother board module. Chapter 2 – Hardware Information...

[Page 28](#) Loosen the four screws and remove the mother board. Put the assembled cushions on the hard disk driver bracket. Chapter 2 – Hardware Information...

[Page 29](#) Lock the HDD onto the cushions with the four screws Chapter 2 – Hardware Information...

[Page 30](#) Connect the SATA cable and power cable into the Hard Disk, and lock in the cable with the cable ties. Connect the SATA cable and the power cable onto the mother board, and lock in the mother board with the four screws. Chapter 2 –...

[Page 31](#) Put the assembled mother board module onto the bottom case, and lock the screw. Put the assembled top case onto the bottom case. Chapter 2 – Hardware Information...

[Page 32](#) 10. Lock the screw. Chapter 2 – Hardware Information...

[Page 33: Mini Pcie Card Installation](#)

Mini PCIe Card Installation Unscrew the Mini PCIe card cover lid. Push the Mini PCIe card into the slot Chapter 2 – Hardware Information...

[Page 34](#) Lock down the Mini PCIe card with the screw. Lock down the Mini PCIe card cover with the screw. Chapter 2 – Hardware Information...

[Page 35: Chapter 3 - Ami Bios Setup](#)

Chapter 3 Chapter 3 – AMI BIOS Setup...

[Page 36: System Test And Initialization](#)

System Test and Initialization These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

[Page 37: Ami Bios Setup](#)

AMI BIOS Setup The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off. To enter BIOS Setup, press ...

[Page 38: Setup Submenu: Main](#)

Setup Submenu: Main Chapter 3 – AMI BIOS Setup...

[Page 39: Setup Submenu: Advanced](#)

Setup Submenu: Advanced Chapter 3 – AMI BIOS Setup...

[Page 40: Advanced: Trusted Computing](#)

3.4.1 Advanced: Trusted Computing Options summary: Security Device Support Disabled Enabled Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. SHA-1 PCR Bank Disabled Enabled Enable or Disable SHA-1 PCR Bank SHA256 PCR Bank Disabled...

[Page 41](#) Storage Hierarchy Disabled Enabled Enable or Disable Storage Hierarchy Endorsement Hierarchy Disabled Enabled Enable or Disable Endorsement Hierarchy TPM2.0 UEFI Spec Version TCG_1_2 TCG_2 Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later Physical Presence Spec Version Select to Tell O.S.

[Page 42: Advanced: Cpu Configuration](#)

3.4.2 Advanced: CPU Configuration Options summary: Intel Virtualization Technology Disabled Enabled When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology VT-d Disabled Enabled Enable/Disable CPU VT-d EIST Disabled Enabled Enable/Disable Intel SpeedStep Power Limit 1 Enable Disabled Enabled Enable/Disable Power Limit 1...

[Page 43: Advanced: Sata Drives](#)

3.4.3 Advanced: SATA Drives Options summary : Chipset SATA Disabled Enabled Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port). Chapter 3 – AMI BIOS Setup...

[Page 44: Advanced: Usb Configuration](#)

3.4.4 Advanced: USB Configuration Options summary : Legacy USB Support Disabled Enabled Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications. Chapter 3 – AMI BIOS Setup...

[Page 45: Advanced: Hardware Monitor](#)

3.4.5 Advanced: Hardware Monitor Options summary: System Fan Smart Control Disabled Enabled For En/Disable Fan 1 Smart Control. Enabled: FAN is running in accordance with user settings. Disabled: FAN is always running with full speed Fan Control Mode Automatic Mode Manual Mode Manual Mode: Depends on PWM Duty.

[Page 46](#) Full Speed Temperature Temperature Limit Value of FAN Full Speed PWM Slope 5 (1-15) Slope PWM value/Degree C for FAN Speed Control Range:[1-15] Chapter 3 – AMI BIOS Setup...

[Page 47: Advanced: Sio Configuration](#)

3.4.6 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

[Page 48: Sio Configuration: Serial Port Configuration](#)

3.4.6.1 SIO Configuration: Serial Port Configuration Options summary: Use This Device Disabled Enabled Enable or Disable this Logical Device. Possible: Use Automatic Settings IO=2F8h; IRQ=3; IO=3F8h; IRQ=4; Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.

[Page 49](#) 3.4.6.1.1 Serial Port Configuration: Serial Port Console Redirection Options summary: Console Redirection Disabled Enabled Console Redirection Enabled or Disabled. Chapter 3 – AMI BIOS Setup...

[Page 50: Console Redirection Settings](#)

3.4.6.1.2 Console Redirection Settings Options summary: Terminal Type VT100 VT100+ VT-UTF8 ANSI Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. Bits per second 9600 19200...

[Page 51](#) Parity None Even Mark Space A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd.

[Page 52](#) The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS. Chapter 3 – AMI BIOS Setup...

[Page 53](#) 3.4.6.1.3 Serial Port for Out-of-Band Management/Windows Emergency Management Services(EMS) Options summary: Terminal Type VT100 VT100+ VT-UTF8 ANSI VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.

[Page 54](#) Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

[Page 55](#) 3.4.6.1.4 LAN Bypass Configuration Options summary : STATUS LED CTRL LED OFF RED LED ON RED LED BLINK RED LED FAST BLINK GREEN LED ON GREEN LED BLINK GREEN LED

FAST BLINK Configure LAN Bypass Status LED. LAN kit Power ON Bypass PassTru Setting LAN kit function behavior when power on.(Bypass/Pass Through)

[Page 56](#) WDT configuration Force Bypass SystemReset Configure WDT behavior , System Reset Force Bypass Chapter 3 – AMI BIOS Setup...

[Page 57: Advanced: Power Management](#)

3.4.7 Advanced: Power Management Options summary: Power Mode ATX Type AT Type Select Power Supply Mode. Restore AC Power Loss Power Off Power On Last State Select AC power state when power is re-applied after a power failure. RTC Wake system from S5 Disabled Fixed time Dynamic time...

[Page 58](#) Wake up minute (Fixed time option) 0-59 Wake up second (Fixed time option) 0-59 Wake up minute increase (Dynamic time option) Chapter 3 – AMI BIOS Setup...

[Page 59: Digital Io Port Configuration](#)

3.4.8 Digital IO Port Configuration DIO_P#1~4 Input Output Set DIO as Input or Output DIO_P#5~8 Input Output Set DIO as Input or Output DIO_P#1~4 Direction High Set output level when DIO pin is output Chapter 3 – AMI BIOS Setup...

[Page 60: Setup Submenu: Chipset](#)

Setup submenu: Chipset Chapter 3 – AMI BIOS Setup...

[Page 61: Chipset: North Bridge](#)

3.5.1 Chipset: North Bridge Options summary: Primary Display PCIe Select which of IGD/PCI Graphics device should be Primary Display Chapter 3 – AMI BIOS Setup...

[Page 62: North Bridge: Ami Graphic Output Protocol Policy](#)

3.5.1.1 North Bridge: AMI Graphic Output Protocol Policy Options summary : Output Select HDMI1 Output Interface Chapter 3 – AMI BIOS Setup...

[Page 63: Setup Submenu: Security](#)

Setup submenu: Security Change User/Supervisor Password You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility. If you highlight these items and press Enter, a dialog box appears which lets you enter a password.

[Page 64: Setup Submenu: Boot](#)

Setup submenu: Boot Options summary : Quiet Boot Disabled Enabled Enables or disables Quiet Boot option. Network Stack Disabled Enabled Enable/Disable UEFI Network Stack Chapter 3 – AMI BIOS Setup...

[Page 65: Setup Submenu: Exit](#)

Setup submenu: Exit Chapter 3 – AMI BIOS Setup...

[Page 66: Chapter 4 - Driver Installation](#)

Chapter 4 Chapter 4 – Driver Installation...

[Page 67: Driver Installation](#)

Driver Installation Please download the driver from AAEON website. It contains all the drivers and utilities you need to setup your product. Follow the steps below to install the drivers.
<http://www.aaeon.com/en/p/desktop-network-appliance-fws-2273> Step 1 - Open the Step 1 - LAN folder and select the OS folder your system is. Step 2 -...

[Page 68: Appendix A - Watchdog Timer Programming](#)

Appendix A Appendix A – Watchdog Timer Programming...

[Page 69: Watchdog Timer Initial Program](#)

Watchdog Timer Initial Program Table 1 : SuperIO relative register table Default Value Note SIO MB PnP Mode Index Register Index 0x2E(Note1) 0x2E or 0x4E SIO MB PnP Mode Data Register Data 0x2F(Note2) 0x2F or 0x4F Table 2 : Watchdog relative register table Register BitNum Value...

[Page 70](#) *****

```
// SuperIO relative definition (Please reference to Table 1) #define byte SIOIndex //This parameter is represented from Note1 #define byte SIOData //This parameter is represented from Note2 #define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte IOPort); // Watch Dog relative definition (Please reference to Table 2) #define byte TimerLDN //This parameter is represented from Note3 #define byte TimerReg //This parameter is represented from Note4 #define byte TimerVal // This parameter is represented from Note24...
```

[Page 71](#) *****

```
VOID Main() { // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) // (boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure : AaeonWDTEnable // This procedure will enable the WDT counting. AaeonWDTEnable(); ***** Appendix A - Watchdog Timer Programming...
```

[Page 72](#) *****

```
// Procedure : AaeonWDTEnable VOID AaeonWDTEnable () { WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1); // Procedure : AaeonWDTConfig VOID AaeonWDTConfig () { // Disable WDT counting WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0); // Clear Watchdog Timeout Status WDTClearTimeoutStatus(); // WDT relative parameter setting WDTParameterSetting(); VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value) { SIOBitSet(LDN, Register, BitNum, Value);...
```

[Page 73](#) *****

```
VOID SIOEnterMBPnPMode() { Switch(SIOIndex) { Case 0x2E: IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x01); IOWriteByte(SIOIndex, 0x55); IOWriteByte(SIOIndex, 0x55); Break; Case 0x4E: IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x01); IOWriteByte(SIOIndex, 0x55); IOWriteByte(SIOIndex, 0xAA); Break; VOID SIOExitMBPnPMode() { IOWriteByte(SIOIndex, 0x02); IOWriteByte(SIOData, 0x02); VOID SIOSelectLDN(byte LDN) { IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN);...
```

[Page 74](#) *****

```
VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value) { Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData); TmpValue &= ~(1 << BitNum); TmpValue |= (Value << BitNum); IOWriteByte(SIOData, TmpValue); SIOExitMBPnPMode(); VOID SIOByteSet(byte LDN, byte Register, byte Value) { SIOEnterMBPnPMode();...
```

[Page 75: Appendix B - I/O Information](#)

Appendix B Appendix B - I/O Information...

[Page 76: I/O Address Map](#)

I/O Address Map Appendix B - I/O Information...

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[Page 78: Memory Address Map](#)

Memory Address Map Appendix B - I/O Information...

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[Page 80: Irq Mapping Chart](#)

IRQ Mapping Chart Appendix B - I/O Information...

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[Page 89: Appendix C - Standard Lan Bypass Platform Setting](#)

Appendix C Appendix C – Standard LAN Bypass Platform Setting...

[Page 90: Introduction To Led](#)

Introduction to LED FWS-2273 provides a LED indicator which can change the LED status by AAEON SDK. User is able to program the LED status to express different status. Appendix C – Standard LAN Bypass Platform Setting...

[Page 91: Status Led Configuration](#)

C.1.1 Status LED Configuration The LED status indicator of FWS-2273 is programmable with AAEON SDK for your application. Table1: LED Status STA_LED2 STA_LED1 STA_LED0 LED Off Red Blinking (Slowly) Red Blinking (Quickly) Reserved Green Blinking (Slowly) Green Blinking (Quickly) Green Table2: Status LED and register mapping table CPLD Slave Address 0x90 (Note1) Attribute...

[Page 92: Sample Code](#)

C.1.2 Sample Code

```
*****
#define Byte CPLD_SLAVE_ADDRESS //This parameter is represented from Note1 #define Byte
OFFSET //This parameter is represented from Note2
*****
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET); switch( LED_FLAG) case 0:
//LED Off //BIT2=0, BIT1=0, BIT0=0 bData = bData & 0xF8; break;...
```

[Page 93](#) //Green LED On //BIT2=1, BIT1=1, BIT0=1 bData = (bData & 0xF8) | 0x07; break;
case 5: //Green LED Blink //BIT2=1, BIT1=0, BIT0=1 bData = (bData & 0xF8) | 0x05; break; case
6: //Green LED Fast Blink //BIT2=1, BIT1=1, BIT0=0 bData = (bData & 0xF8) | 0x06; break;...

[Page 94: Introduction To Lan Bypass](#)

C.2 Introduction to LAN Bypass FWS-2273 provides LAN Bypass kit and allow uninterrupted network traffic even if a single in-line appliance is shut down or hangs. Appendix C – Standard LAN Bypass Platform Setting...

[Page 95: Lan Bypass](#)

C.2.1 LAN Bypass Table1: LAN Kit ID Select LAN_ID2 LAN_ID1 LAN_ID0 LAN kit selected LAN Kit 1 Selected LAN Kit 2 Selected Table2: LAN Bypass register table Function Description LAN_ID3 Use for selecting which LAN kit will be LAN_ID2 configured, refer to Table 1 of ID Select table of LAN kit.

[Page 96](#) Table3: LAN Bypass register mapping table CPLD Slave Address 0x90 (Note1) Attribute Offset(SMBUS) BitNum Value LAN_ID3 0x01(Note2) (Table 1) LAN_ID2 0x01(Note2) (Table 1) LAN_ID1 0x01(Note2) (Table 1) LAN_ID0 0x01(Note2) (Table 1) PWR_ON 0x01(Note2) (Table 2) PWR_OFF 0x01(Note2) (Table 2) WDT_EN 0x01(Note2) (Table 2) ACT_EN...

[Page 97: Sample Code](#)

C.2.2 Sample Code

```
*****  
#define Byte CPLD_SLAVE_ADDRESS //This parameter is represented from Note1 #define Byte  
OFFSET //This parameter is represented from Note2  
***** //  
Select Lan Pair BYTE bLanSel = LAN_PAIR; BYTE bData =  
SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET); // Set Reg01h bit3 if(bLanSel &...
```

[Page 98](#) bData = bData & 0xDF; else // Bypass bData = bData | 0x20; // WDT Action (Reg01h
bit4) if(SET_WDT_RESET) // Reset bData = bData & 0xEF; else // Bypass bData = bData | 0x10;
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData); // Apply Settings (Reg01h bit7) bData
= SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);...

[Page 99: Introduction To Software Reset Button Configuration](#)

C.3 Introduction to Software Reset Button Configuration FWS-2273 provides a general propose
input button which status get by AAEON SDK. Appendix C - Standard LAN Bypass Platform
Setting...

[Page 100: Soft Reset Button Configuration](#)

C.3.1 Soft Reset Button Configuration Table 2 : LAN Bypass relative register table Function
Description Reading this register returns the pin level status which is normal high active low.
BTN_STS 0: Pin Level States Low. 1: Pin Level States High. Table 1 : Soft Reset Button register
mapping table Attribute Register(I/O)

[Page 101: Sample Code](#)

C.3.2 Sample Code

```
***** #define  
Word BTN_STS //This parameter is represented from Note1 #define Byte BTN_STS_R //This  
parameter is represented from Note2  
***** Byte  
GET_Value (Word IoAddr, Byte BitNum,Byte Value){ BYTE TmpValue; TmpValue = inportb  
(IoAddr); return (TmpValue & (1 << BitNum))  
***** VOID  
Main(){ Byte RstBtn;...
```

This manual is also suitable for:

[Aaeon fws-2273](#)