



Asus AAEON GENE-WHU6 User Manual

3.5" subcompact board

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Summary of Contents for Asus AAEON GENE-WHU6

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[Page 3](#) Acknowledgements All other products' name or trademarks are properties of their respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. • Intel® and Celeron® are registered trademarks of Intel Corporation • Intel Core™ are trademarks of Intel

[Page 4](#) Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity GENE-WHU6 MB Heatspreader If any of these items are missing or damaged, please contact your distributor or sales representative immediately. Preface...

[Page 5](#) About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the product page at AAEON.com for the latest version of this document.

[Page 6](#) Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

[Page 7](#) If any of the following situations arises, please contact our service personnel:
Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

[Page 8](#) FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

[Page 9](#) China RoHS Requirements (CN) AAEON Main Board/ Daughter Board/ Backplane (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) ...

[Page 10](#) China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Main Board/ Daughter Board/ Backplane Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg)

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Chapter 1 Chapter 1 - Product Specifications...

[Page 16: Specifications](#)

1.1 Specifications System Form Factor 3.5" Subcompact Board CPU Intel® 8th Generation Core™/ Celeron Processor: Core i7-8665UE (4C/8T, 1.70GHz, up to 4.40GHz) Core i5-8365UE (4C/8T, 1.60GHz, up to 4.10GHz) Core i3-8145UE (2C/4T, 2.20GHz, up to 3.90GHz) Celeron®...

[Page 17](#) Power Requirement +9 ~ 36V (Optional: +12V) Power Supply Type AT/ATX

Connector Phoenix 2-pin Connector Power Consumption (Typical) 4.83A at +12V with Intel® i7-8665UE, DDR4L 2400MHz 16GB memory Power Consumption (Max) 7.30A at +12V with Intel®...

[Page 18](#) External I/O Ethernet Intel® i210/i211 & i219, 10/100/1000 Base, RJ-45 x 2 USB3.2 Gen 2 x 4 Serial Port — Video HDMI 2.0a x 1 VGA x 1 Internal I/O USB2.0 x 2 Serial Port COM1 (RS232/422/485, supports RI) COM2 (RS232/422/485, supports 5V/12V/RI)

[Page 19](#) Expansion M.2 (Continued) E-Key M.2 2230 x 1 (PCIe, USB2.0) BIO — Environmental Operating Temperature 32°F ~ 140°F (0°C ~ 60°C) Storage Temperature -40°F ~ 176°F (-40°C ~ 80°C) Operating Humidity 0% ~ 90% relative humidity, non-condensing MTBF (Hours) 354,194 EMC Certification...

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1.2 Block Diagram Chapter 1 – Product Specifications...

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Dimensions Chapter 2 – Hardware Information...

[Page 23: Jumpers And Connectors](#)

2.2 Jumpers and Connectors Chapter 2 – Hardware Information...

[Page 24: List Of Jumpers](#)

2.3 List of Jumpers Please refer to the table below for all of the board's jumpers that you can configure for your application Label Function JP 1 Front Panel Connector JP 3 COM2 Pin8 Function Selection LVDS/eDP Port Backlight Inverter VCC Selection and Operating VDD JP 4 Selection JP 5...

[Page 25: Com2 Pin8 Function Selection \(Jp3\)](#)

2.3.2 COM2 Pin8 Function Selection (JP3) Ring (Default) +12V 2.3.3 LVDS/eDP Port Backlight Inverter VCC and VDD Selection (JP4) VCC Selection VDD Selection +12V +5V (Default) +3.3V (Default) Note: JP4 Default is two (2) jumpers placed on pins 3-5 and pins 2-4. 2.3.4 LVDS/eDP Port Backlight Lightness Control Mode Selection (JP5) 1 2 3...

[Page 26: Clear Cmos Jumper \(Jp9\)](#)

2.3.6 Clear CMOS Jumper (JP9) Normal (Default) Clear CMOS 2.3.7 Auto Power Button Enable/Disable Selection (JP10) Disable/ATX Enable/AT (Default) Chapter 2 – Hardware Information...

[Page 27: List Of Connectors](#)

2.4 List of Connectors Please refer to the table below for all of the board's connectors that you can configure for your application Label Function CN 1 +5V Output for SATA HDD CN 2 SATA Port CN 3 External Power Input CN 5 Audio I/O Port...

[Page 28: Output For Sata Hdd \(Cn1\)](#)

Label Function CN 25 LAN (RJ-45) Port1 CN 26 Dual USB3.1 Port 0/Port 1 CN 27 Dual USB3.1 Port 2/Port 3 CN 28 HDMI Connector CN 29 VGA Port CN 30 M.2 B-Key 2280 CN 31 LAN SDP CONN 2.4.1 +5V Output for SATA HDD (CN1) Pin...

[Page 29: Sata Port \(Cn2\)](#)

2.4.2 SATA Port (CN2) Pin Pin Name Signal Type Signal Level SATA_TX+ DIFF SATA_TX- DIFF SATA_RX- DIFF SATA_RX+ DIFF 2.4.3 External Power Input (CN3) Pin Pin Name Signal Type Signal Level +12V +9~+36V (or +12V) at 8A Note: There are two types of power input, 9~36V or 12V (by BOM option).

[Page 30: Audio I/O Port \(Cn5\)](#)

2.4.4 Audio I/O Port (CN5) P in P in Name Sig nal Type Sig nal Level MIC_L MIC_R GND_AUDIO LINE_L_IN LINE_R_IN GND_AUDIO LEFT_OUT GND_AUDIO RIGHT_OUT +5V_AUDIO Chapter 2 – Hardware Information...

[Page 31: External +5Vsb Input \(Cn6\)](#)

2.4.5 External +5VSB Input (CN6) P in P in Name Sig nal Type Sig nal Level PS_ON# +5VSB +5V at 2A 2.4.6 DDR SO-DIMM Slot (CN7) Standard Specifications Chapter 2 – Hardware Information...

[Page 32: Com Port 1 \(Cn8\)](#)

2.4.7 COM Port 1 (CN8) R S-232 P in P in Name Sig nal Type Sig nal Level DCD1 DSR1 RTS1 ±5V ±5V CTS1 DTR1 ±5V Chapter 2 – Hardware Information...

[Page 33](#) R S-485 P in P in Name Sig nal Type Sig nal Level RS485_D- ±5V RS485_D+ ±5V R S-422 P in P in Name Sig nal Type Sig nal Level RS422_TX- ±5V RS422_TX+ ±5V RS422_RX+ RS422_RX- Chapter 2 – Hardware Information...

[Page 34: Com Port 2 \(Cn9\)](#)

2.4.8 COM Port 2 (CN9) R S-232 P in P in Name Sig nal Type Sig nal Level DCD2 DSR2 RTS2 ±5V ±5V CTS2 DTR2 ±5V Chapter 2 – Hardware Information...

[Page 35](#) R S-485 P in P in Name Sig nal Type Sig nal Level RS485_D2- ±5V RS485_D2+ ±5V NC/+5V/+12V +5V/+12V at 0.5A R S-422 P in P in Name Sig nal Type Sig nal Level RS422_TX2- ±5V RS422_TX2+ ±5V RS422_RX2+ RS422_RX2- NC/+5V/+12V +5V/+12V at 0.5A...

[Page 36: Mini- Card Slot \(Full-Mini Card\) \(Cn10\)](#)

2.4.9 Mini-Card Slot (Full-Mini Card) (CN10) P in P in Name Sig nal Type Sig nal Level PCIE_WAKE# +3.3VSB +3.3V +1.5V +1.5V PCIE_CLK_REQ# UIM_PWR UIM_DATA PCIE_REF_CLK- DIFF UIM_CLK PCIE_REF_CLK+ DIFF UIM_RST UIM_VPP W_DISABLE# +3.3V PCIE_RST# +3.3V PCIE_RX- DIFF +3.3VSB +3.3V...

[Page 37](#) P in P in Name Sig nal Type Sig nal Level PCIE_RX+ DIFF +1.5V +1.5V SMB_CLK +3.3V PCIE_TX- DIFF SMB_DATA +3.3V PCIE_TX+ DIFF USB_D- DIFF USB_D+ DIFF +3.3VSB +3.3V +3.3VSB +3.3V +1.5V +1.5V Chapter 2 – Hardware Information...

[Page 38: Ddr So-Dimm Slot \(Cn11\)](#)

P in P in Name Sig nal Type Sig nal Level +3.3VSB +3.3V 2.4.10 DDR SO-DIMM Slot (CN11) Standard Specifications 2.4.11 M.2 E-Key 2230 (CN12) Standard Specifications 2.4.12 LVDS/eDP Port Inverter /Backlight Connector (CN13) P in P in Name Sig nal Type Sig nal level BKL_PWR...

[Page 39: Lvds/Edp Port \(Cn14\)](#)

2.4.13 LVDS/eDP Port (CN14) Note: LVDS LCD_PWR can be set to +3.3V or +5V by JP4. (See Ch 2.3.3) Note: LVDS LCD_PWR supports current of 2A P in LVDS Sig nal Type Sig nal Level BKL_ENABLE BKL_ENABLE BKL_CONTROL...

[Page 40](#) P in LVDS Sig nal Type Sig nal Level LVDS_DA2- eDP_TXN0 DIFF LVDS_DA2+ eDP_TXP0 DIFF LVDS_DA3- DIFF LVDS_DA3+ eDP_HPD DIFF DDCC_DATA eDP_AUX_N +3.3V DDCC_CLK eDP_AUX_P +3.3V LVDS_DB0- DIFF LVDS_DB0+ DIFF LVDS_DB1- DIFF LVDS_DB1+ DIFF LVDS_DB2- DIFF LVDS_DB2+ DIFF LVDS_DB3- DIFF LVDS_DB3+ DIFF LCD_PWR...

[Page 41: Usb 2.0 Port 5 \(Cn15\)](#)

2.4.14 USB 2.0 Port 5 (CN15) P in P in Name Sig nal Type Sig nal Level +5VSB +5V at 0.5A USB5_D- DIFF USB5_D+ DIFF 2.4.15 BIOS Debug Port (CN16) P in P in Name Sig nal Type Sig nal Level SPI_MISO SPI_CLK Chapter 2 –...

[Page 42: Usb 2.0 Port 6 \(Cn17\)](#)

P in P in Name Sig nal Type Sig nal Level +3.3VSB +3.3V SPI_MOSI SPI_CS 2.4.16 USB 2.0 Port 6 (CN17) P in P in Name Sig nal Type Sig nal Level +5VSB +5V at 0.5A USB6_D- DIFF USB6_D+

DIFF G ND 2.4.17 LPC Port (CN18)

[Page 43: Digital I/O Port \(Cn19\)](#)

P in P in Name Sig nal Type Sig nal Level +3.3V +3.3V LFRAME# LRESET# +3.3V LCLK
SMB_DATA/I2C_SDA SMB_CLK/I2C_CLK SMB_ALERT/SERIRQ +3.3V 2.4.18 Di gital I/O Port (CN19)
P in Sig nal Description P in Sig nal Description +V5S (0.5A) Chapter 2 – Hardware Information...

[Page 44: Nano Sim Card Socket \(Cn20\)](#)

2.4.19 Nano SIM Card Socket (CN20) P in P in Name Sig nal Type Sig nal Level UIM_PWR
UIM_RST UIM_CLK UIM_VPP UIM_DATA Chapter 2 – Hardware Information...

[Page 45: Touchscreen Connector \(Optional\) \(Cn21\)](#)

2.4.20 Touchscreen Connector (Optional) (CN21) N o te: Touch mode can be set by BIOS. 8- W
ire P in P in Name Sig nal Type Sig nal Level TOP EXCITE BOTTOM EXCITE LEFT EXCITE RIGHT
EXCITE TOP SENSE BOTTOM SENSE LEFT SENSE RIGHT SENSE...

[Page 46](#) 4- W ire P in P in Name Sig nal Type Sig nal Level BOTTOM LEFT RIGHT 5- W ire P in P
in Name Sig nal Type Sig nal Level Chapter 2 – Hardware Information...

[Page 47: Cpu Fan \(Cn22\)](#)

5- W ire P in P in Name Sig nal Type Sig nal Level UL(Y) UR(H) LL(L) LR(X) SENSE(S) 2.4.21 CPU
Fan (CN22) P in P in Name Sig nal Type Sig nal Level FAN_POWER +12V at 1A FAN_TAC N o te:
Max. driving current is 1A Chapter 2 –...

[Page 48: Battery Connector \(Cn23\)](#)

2.4.22 Battery Connector (CN23) P in P in Name Sig nal Type Sig nal level +3.3V 3.3V 2.4.23 L
AN (RJ-45) Port 1 /Port 2 (CN24/CN25) P in P in Name Sig nal Type Sig nal level MDIO+ DIFF
MDIO-...

[Page 49: Usb 3.2 Gen 2 Ports 0 & 1 \(Cn26\)](#)

2.4.24 USB 3.2 Gen 2 Ports 0 & 1 (CN26) P in P in Name Sig nal Type Sig nal Level +5VSB +5V
at 0.9A USB0_D- DIFF USB0_D+ DIFF USB0_SSRX- DIFF USB0_SSRX+ DIFF USB0_SSTX- DIFF
USB0_SSTX+ DIFF +5VSB +5V at 0.9A USB1_D- DIFF USB1_D+...

[Page 50: Usb 3.2 Gen 2 Ports 2 & 3 \(Cn27\)](#)

2.4.25 USB 3.2 Gen 2 Ports 2 & 3 (CN27) P in P in Name Sig nal Type Sig nal Level +5VSB +5V
at 0.9A USB2_D- DIFF USB2_D+ DIFF USB2_SSRX- DIFF USB2_SSRX+ DIFF USB2_SSTX- DIFF
USB2_SSTX+ DIFF +5VSB +5V at 0.9A USB3_D- DIFF USB3_D+...

[Page 51: Hdmi \(Cn28\)](#)

2.4.26 HDMI (CN28) P in P in Name Sig nal Type Sig nal Level HDMI_TX2+ DIFF HDMI_TX2- DIFF
HDMI_TX1+ DIFF HDMI_TX1- DIFF HDMI_TX0+ DIFF HDMI_TX0- DIFF HDMI_CLK+ DIFF HDMI_CLK-
DIFF DDC_CLK DDC_DATA HDMI_HPD Chapter 2 – Hardware Information...

[Page 52: Vga Port \(Cn29\)](#)

2.4.27 VG A Port (CN29) P in P in Name Sig nal Type Sig nal Level GREEN BLUE RED_GND RTN
GREEN_GND RTN BLUE_GND RTN DDC_DATA HSYNC VSYNC DDC_CLK 2.4.28 M.2 B-Key 2280
(CN30) Standard Specifications Chapter 2 – Hardware Information...

[Page 53: Lan Spd Connector \(Cn31\)](#)

2.4.29 L AN SPD Connector (CN31) P in P in Name Sig nal Type Sig nal Level SDP0 SDP1 SDP2
SDP3 Chapter 2 – Hardware Information...

[Page 54: Thermal Solutions](#)

2.5 T he rmal Solutions 2.5.1 G E NE-WHU6-FAN01 Single piece cooler, does not require use of
heat spreader Chapter 2 – Hardware Information...

[Page 55](#) G E NE-WHU6-FAN01 Assembly Chapter 2 – Hardware Information...

[Page 56: Gene-Whu6-Fan02](#)

2.5.2 G E NE-WHU6-FAN02 Single piece cooler, does not require use of heat spreader. Chapter 2 – Hardware Information...

[Page 57](#) GEN E-WHU6-FAN02 Assembly Chapter 2 – Hardware Information...

[Page 58: Gene-Whu6-Hsk01](#)

2.5.3 G E NE-WHU6-HSK01 Single piece heatsink, does not require use of heat spreader. Note: Use only with Intel Core i3 and Celeron processors. Chapter 2 – Hardware Information...

[Page 59](#) GEN E-WHU6-HSK01 Assembly Chapter 2 – Hardware Information...

[Page 60: Gene-Whu6-Hsk02](#)

2.5.4 G E NE-WHU6-HSK02 Chapter 2 – Hardware Information...

[Page 61](#) Heat Spreader with Heatsink Cover Chapter 2 – Hardware Information...

[Page 62: Gene-Whu6-Hsk03](#)

2.5.5 G E NE-WHU6-HSK03 Single piece heatsink, does not require use of heat spreader. Note: Limited to use with less than 0.5 m/s airflow. Chapter 2 – Hardware Information...

[Page 63](#) GEN E-WHU6-HSK03 Assembly Chapter 2 – Hardware Information...

[Page 64: Chapter 3 - Ami Bios Setup](#)

Chapter 3 Chapter 3 - AMI BIOS Setup...

[Page 65: System Test And Initialization](#)

System Test and Initialization The GENE-WHU6 board uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the module will output a few short beeps or display an error message. The module can usually continue the boot up sequence with non-fatal errors.

[Page 66: Ami Bios Setup](#)

3.2 AMI BIOS Setup The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off. To enter BIOS Setup, press ...

[Page 67: Setup Submenu: Main](#)

3.3 Setup Submenu: Main Chapter 3 – AMI BIOS Setup...

[Page 68: Setup Submenu: Advanced](#)

3.4 Setup Submenu: Advanced Chapter 3 – AMI BIOS Setup...

[Page 69: Trusted Computing](#)

3.4.1 Trusted Computing Options Summary Security Device Support Disable Enable Optimal Default, Failsafe Default Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. SHA-1 PCR Bank Disable Enable Optimal Default, Failsafe Default...

[Page 70](#) Options Summary Platform Hierarchy Disabled Enabled Optimal Default, Failsafe Default Enable or disable Platform Hierarchy Storage Hierarchy Disabled Enabled Optimal Default, Failsafe Default Enable or Disable Storage Hierarchy Endorsement Hierarchy Disabled Enabled Optimal Default, Failsafe Default Enable or Disable Endorsement Hierarchy TPM 2.0

[Page 71: Cpu Configuration](#)

3.4.2 CPU Configuration Op tions Summary Hyp er-Threading Disabled Enabled Optimal Default, Failsafe Default Enable/Disable Hyper-Threading Technology A ctive Processor Cores Optimal Default, Failsafe Default Number of cores to enable in each processor package. I nt el (VMX) Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default...

[Page 72](#) Op tions Summary Turbo Mode Disabled Enabled Optimal Default, Failsafe Default Enable/Disable Turbo mode Chapter 3 – AMI BIOS Setup...

[Page 73: Sata Configuration](#)

3.4.3 SATA Configuration Op tions Summary SATA Controller(s) Disabled Enabled Optimal Default, Failsafe Default Enable/Disable SATA Device. SATA GEN SPEED Auto Optimal Default; Failsafe Default GEN1 GEN2 GEN3 SATA GEN SPEED SELECTION mSATA port Disabled Enabled Optimal Default, Failsafe Default Enable or Disable SATA Port Po rt * Disabled...

[Page 74: Hardware Monitor](#)

3.4.4 Hardware Monitor Op tions Summary Smart Fan Disabled Enabled Optimal Default; Failsafe Default Enable or Disable Smart Fan Chapter 3 – AMI BIOS Setup...

[Page 75: Smart Fan Mode Configuration](#)

3.4.4.1 Sm ar t Fan Mode Configuration A uto Duty Cycle Mode Op tions Summary FAN1 Output Output PWM mode (open drain) mo de Linear Fan Application Optimal Default, Failsafe Default Output PWM mode (push pull) FAN1 Output mode select: Output PWM mode (push pull) to control 4-wire fans.

[Page 76](#) Manual Duty Mode Op tions Summary Manual Duty Mode Optimal Default, Failsafe Default Manual mode fan control, user can write expected duty cycle (PWM fan type) 1-100 Chapter 3 – AMI BIOS Setup...

[Page 77: Sio Configuration](#)

3.4.5 SIO Configuration Chapter 3 – AMI BIOS Setup...

[Page 78: Serial Port 1 Configuration](#)

3.4.5.1 Se ri al Port 1 Configuration Op tions Summary U s e This Device Disable Enable Optimal Default, Failsafe Default Enable or Disable this Logical Device. Po ssible: Use Automatic Settings Optimal Default, Failsafe Default IO=3F8h; IRQ=4 IO=2F8h; IRQ=3 Allows user to change Device's Resource settings.

[Page 79: Serial Port 2 Configuration](#)

3.4.5.2 Se ri al Port 2 Configuration Op tions Summary U s e This Device Disable Enable Optimal Default, Failsafe Default Enable or Disable this Logical Device. Po ssible: Use Automatic Settings Optimal Default, Failsafe Default IO=2F8h; IRQ=3 IO=3F8h; IRQ=4 Allows user to change Device's Resource settings.

[Page 80: Power Management](#)

3.4.6 Powe r Management Op tions Summary Po wer Mode ATX Type Optimal Default, Failsafe Default AT Type Select system power mode R estore AC Power Last State Optimal Default, Failsafe Default Lo s s Always On Always Off IO Restore AC power Loss R TC wake system Disable Optimal Default, Failsafe Default...

[Page 81: Digital Io Port Config Uration](#)

3.4.7 Di gital IO Port Configuration Op tions Summary GP I* Output Input Set DIO as Input or Output GP O* Output Input Set DIO as Input or Output Out put Level High Optimal Default; Failsafe Default Set output level when DIO pin is output Chapter 3 – ...

[Page 82: Setup Submenu: Chipset](#)

[Page 83: System Agent \(Sa\) Configuration](#)

3.5.1 System Agent (SA) Configuration Chapter 3 – AMI BIOS Setup...

[Page 84: Lvds Panel Configuration](#)

3.5.1.1 LVDS Panel Configuration Options Summary LVDS Disabled Enabled Optimal Default, Failsafe Default Enable/Disable this panel. LVDS Panel Type 640X480@60HZ 800X480@60HZ 800X600@60HZ 1024X600@60HZ 1024X768@60HZ Optimal Default, Failsafe Default 1280X768@60HZ 1280X800@60HZ 1280X1024@60HZ 1366X768@60HZ 1440X900@60HZ 1600X1200@60HZ 1920X1080@60HZ 1920X1200@60HZ Chapter 3 – AMI BIOS Setup...

[Page 85](#) Options Summary Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item. Color Depth 18-bit Optimal Default, Failsafe Default 24-bit 36-bit 48-bit Select color depth Backlight Type Normal Optimal Default, Failsafe Default Inverted Select backlight control signal type Backlight Level Optimal Default, Failsafe Default...

[Page 86](#) Options Summary Center Spreading no spreading Optimal Default, Failsafe Default Depth 0.5% 1.0% 1.5% 2.0% 2.5% Select Center Spreading Depth Chapter 3 – AMI BIOS Setup...

[Page 87: Pch Io Configuration](#)

3.5.2 PCH IO Configuration Options Summary Full-MiniCard Slot SATA Optimal Default, Failsafe Default Function PCIe Select function enabled for Full-MiniCard(CN10) Slot M. 2 KEY-B Slot SATA Function PCIe Optimal Default, Failsafe Default Select function enabled for M.2 KEY-B(CN30) Slot Chapter 3 –...

[Page 88: Serial Io Configuration](#)

3.5.2.1 Serial IO Configuration Options Summary I2C3 Controller Disabled Enabled Optimal Default, Failsafe Default Enables/Disables Serial IO Controller If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.

[Page 89: Setup Submenu: Security](#)

3.6 Setup Submenu: Security Change User/Administrator Password You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

[Page 90: Secure Boot](#)

3.6.1 Secure Boot Options Summary Secure Boot Disabled Optimal Default, Failsafe Default Enabled Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset Secure Boot Mode Custom Optimal Default, Failsafe Default...

[Page 91: Key Management](#)

3.6.1.1 Key Management Options Summary Factory Key Provision Disabled Optimal Default, Failsafe Default Enabled Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset Restore Factory Keys Force System to User Mode.

[Page 92](#) Options Summary Remove 'UEFI CA' from DB Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db) Restore DB defaults Restore DB variable to factory defaults Platform Key(PK) Details Export Update Delete Key Exchange Keys...

[Page 93: Setup Submenu: Boot](#)

3.7 Setup Submenu: Boot Options Summary Quiet Boot Disabled Enabled Optimal Default, Failsafe Default Enable/Disable showing boot logo. Launch PXE ROM Disabled Optimal Default, Failsafe Default Enabled Controls the execution of UEFI Network OpROM Chapter 3 – AMI BIOS

Setup...

[Page 94: Setup Submenu: Save & Exit](#)

3.8 Setup Submenu: Save & Exit Chapter 3 – AMI BIOS Setup...

[Page 95: Chapter 4 - Driver Installation](#)

Chapter 4 Chapter 4 – Driver Installation...

[Page 96: Driver Download/Installation](#)

Driver Download/Installation Drivers for the GENE-WHU6 can be downloaded from the product page on the AAEON website by following this link:
<https://www.aaeon.com/en/p/3and-half-inches-subcompact-boards-gene-bt06> Download the driver(s) you need and follow the steps below to install them . Step 1 – Install Chipset Drivers Open the Step 1 –...

[Page 97](#) Step 4 – Install Serial IO Drivers Open the Step 4 – Intel Serial IO folder and select your OS Run the SetupSerialIO.exe file in the folder Follow the instructions Drivers will be installed automatically Step 5 – Install LAN Driver Open the Step 5 –...

[Page 98: Appendix A - I/O Information](#)

Appendix A Appendix A – I/O Information...

[Page 99: I/O Address Map](#)

I/O Address Map Appendix A – I/O Information...

[Page 100: Memory Address Map](#)

A.2 Memory Address Map Appendix A – I/O Information...

[Page 101: Irq Mapping Chart](#)

A.3 IRQ Mapping Chart Appendix A – I/O Information...

[Page 102](#) Appendix A – I/O Information...

[Page 103: Appendix B - Mating Connectors And Cables](#)

Appendix B Appendix B – Mating Connectors and Cables...

[Page 104](#) Mating Connectors and Cables Mating Connector Connector A available Function Cable P/N Label Cable Vendor Model no +5Vout 2 Pins for CN 1 PHR-2 1702150155 Connector HDD Power SATA CN 2 Molex 88750-5318 SATA Cable 1709070500 Connector +9~24V Vin...

[Page 105](#) Mating Connector Connector A available Function Cable P/N Label Cable Vendor Model no Digital I/O CN 19 Neltron 2026B-10 Connector Touch Screen CN 21 SHR-9V-S-B Connector CPU Fan CN 22 Molex 22-01-2035 Connector External RTC CN 23 Molex 51021-0200...

This manual is also suitable for:

Aaeon gene-whu6-a11-0001Aaeon gene-whu6-a11-0003Aaeon gene-whu6-a11-0004Aaeon gene-whu6-a11-0002