



Asus AAEON COM-SKUC6 User Manual

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Summary of Contents for Asus AAEON COM-SKUC6

[Page 1](#) COM-SKUC6 & COM-KBUC6 COM Express Module User 's Manual 5 Last Updated: October 7, 2021...

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Page 4 Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity COM-SKUC6 or COM-KBUC6 • If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

Page 5 About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the product page at AAEON.com for the latest version of this document.

Page 6 Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references. All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

Page 7 If any of the following situations arises, please contact our service personnel:
 Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

Page 8 FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Page 9 Chi na RoHS Requirements (CN) AAEON Main Board/ Daughter
Board/ Backplane (Pb) (Hg) (C d) (C r(VI)) (PBB) (PBDE)

Page 10 Chi na RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Main Board/ Daughter Board/ Backplane Poisonous or Hazardous Substances or Elements He xavalent Polybrominated Polybrominated C omponent Le ad Me rcury C admium C hromium Biphenyls Diphenyl Ethers (Pb) (Hg)

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Page 14: Chapter 1 - Product Specifications

Chapter 1 Chapter 1 - Product Specifications...

Page 15: Specifications

1.1 Specifications System Form Factor COM Express Compact Size, Type 6 CPU 6th/7th Generation Intel® Core™ U-series Processor CPU Frequency Up to 2.8 GHz, i7-7600U Chip set 6th/7th Generation Intel® Core™ U-series SoC Memory Type DDR3L 1600, SODIMM x1 Max.

Page 16 Di splay VGA /LCD Controller Intel® HD Graphics 520/510 (6th Gen Intel Core) Intel® HD Graphics 620/610 (7th Gen Intel Core) Vid eo Output 3 Simultaneous Displays: Single/Dual Channel LVDS (18/24-bit) or eDP VGA x 1, DDI x 1 (up to 2 x DDI shared with LVDS/eDP) Et

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Chapter 2 Chapter 2 – Hardware Information...

[Page 18: Dimensions, Jumpers And Connectors](#)

Di mensions, Jumpers and Connectors Co mponent Side Chapter 2 – Hardware Information
Component Side...

[Page 19](#) So lder Side Solder Side Chapter 2 – Hardware Information...

[Page 20](#) W it h Heat spreader Chapter 2 – Hardware Information...

[Page 21: List Of Jumpers](#)

2.2 Li st of Jumpers Please refer to the table below for all of the board's jumpers that you can configure for your application Lab el F unction SW 1 AT/ATX switch & DDI/VGA switch DI MM1 DDR3L Socket CN 1 ROW A/B CN 2 ROW C/D...

[Page 22](#) R o w A R o w B P in Sig nal P in Sig nal GBE0_MDI2+ LPC_AD3 GBE0_LINK
GBE0_MDI1- A 10 GBE0_MDI1+ B 10 LPC_CLK A 11 GND (FIXED) B 11 GND (FIXED) A 12
GBE0_MDI0- B 12 PWRBTN# A 13 GBE0_MDI0+ B 13...

[Page 23](#) R o w A R o w B P in Sig nal P in Sig nal A 34 BIOS_DIS0# B 34 I2C_DAT A 35
THRMTRIP# B 35 A 36 USB6- B 36 USB7- A 37 USB6+ B 37 USB7+ A 38 USB_6_7_OC# B 38
USB_4_5_OC#...

[Page 24](#) R o w A R o w B P in Sig nal P in Sig nal A 61 PCIE_TX2+ B 61 PCIE_RX2+ A 62
PCIE_TX2- B 62 PCIE_RX2- A 63 GPI1 B 63 GPO3 A 64 PCIE_TX1+ B 64 PCIE_RX1+ A 65
PCIE_TX1- B 65...

[Page 25](#) R o w A R o w B P in Sig nal P in Sig nal A 88 PCIE0_CK_REF+ B 88 BISO_DIS1# A 89
PCIE0_CK_REF- B 89 VGA_RED A 90 GND (FIXED) B 90 GND (FIXED) A 91 +V3.3S(option) B 91
VGA_GRN A 92 SPI_MISO...

[Page 26: Row C/D Connector \(Cn2\)](#)

2.2 .3 ROW C/D Connector (CN2) R o w C R o w D P in Sig nal P in Sig nal GND (FIXED) GND
(FIXED) GND (FIXED) GND (FIXED) USB_SSRX0- USB_SSTX0- USB_SSRX0+ USB_SSTX0+ GND
(FIXED) GND (FIXED) USB_SSRX1- USB_SSTX1- USB_SSRX1+ USB_SSTX1+ GND (FIXED)

[Page 27](#) R o w C R o w D P in Sig nal P in Sig nal RSVD DDI1_PAIR0+ RSVD DDI1_PAIR0- RSVD
RSVD DDI1_PAIR1+ DDI1_PAIR1- GND (FIXED) GND (FIXED) DDI2_CTRLCLK_AUX+ DDI1_PAIR2+
DDI2_CTRLDATA_AUX- DDI1_PAIR2- DDI2_DDC_AUX_SEL DDI1_DDC_AUX_SEL RSVD RSVD
DDI1_PAIR3+ DDI1_PAIR3- RSVD DDI2_PAIR0+ DDI2_PAIR0- GND (FIXED) GND (FIXED)

[Page 28](#) R o w C R o w D P in Sig nal P in Sig nal GND (FIXED) GND (FIXED) RSVD RSVD RSVD
RSVD RSVD GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND
(FIXED) RSVD RSVD Chapter 2 –...

[Page 29](#) R o w C R o w D P in Sig nal P in Sig nal GND (FIXED) GND (FIXED) RSVD RSVD GND
(FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND (FIXED) GND
(FIXED) RSVD RSVD C100 GND (FIXED) D100...

[Page 30: Rtc Connector \(Cn3\)](#)

R o w C R o w D P in Sig nal P in Sig nal C106 VCC_12V D106 VCC_12V C107 VCC_12V D107
VCC_12V C108 VCC_12V D108 VCC_12V C109 VCC_12V D109 VCC_12V C110 GND (FIXED) D110
GND (FIXED) *Note Custom BIOS require to active this pin. This function for i5/i7 sku CPU o nly.
2.2 .4 RTC Connector (CN3) P in...

[Page 31: Function Block Diagram](#)

[Page 32: Chapter 3 - Ami Bios Setup](#)

Chapter 3 Chapter 3 - AMI BIOS Setup...

[Page 33: System Test And Initialization](#)

System Test and Initialization The board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

[Page 34: Ami Bios Setup](#)

3.2 AMI BIOS Setup The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off. To enter Setup, power on the computer and press or <ESC>...

[Page 35: Setup Submenu: Main](#)

3.3 Setup submenu: Main Chapter 3 – AMI BIOS Setup...

[Page 36: Setup Submenu: Advanced](#)

3.4 Setup submenu: Advanced Chapter 3 – AMI BIOS Setup...

[Page 37: Advanced: Cpu Configuration](#)

3.4.1 Advanced: CPU Configuration Options Summary Hyper-Threading Disabled Enabled Optimal Default, Failsafe Default Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). Intel (VMX) Disabled Virtualization Enabled...

[Page 38: Advanced: Sata Configuration](#)

3.4.2 Advanced: SATA Configuration Options Summary SATA Controller(s) Enabled Optimal Default, Failsafe Default Disabled Enable/Disable SATA Device. SATA Controller Auto Optimal Default, Failsafe Default Speed Gen1 Gen2 Gen3 Indicates the maximum speed the SATA controller can support. Port 0 Disabled Enabled Optimal Default, Failsafe Default...

[Page 39](#) Options Summary Port 1 Disabled Enabled Optimal Default, Failsafe Default Enable or Disable SATA Port. Hot Plug Disabled Optimal Default, Failsafe Default Enabled Designates this port as Hot Pluggable. Port 2 Disabled Enabled Optimal Default, Failsafe Default Enable or Disable SATA Port.

[Page 40: Advanced: Usb Configuration](#)

3.4.3 Advanced: USB Configuration Options summary: Options Summary Legacy USB Support Enabled Optimal Default, Failsafe Default Disabled Auto Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI application. Chapter 3 –...

[Page 41: Advanced: On-Module Features](#)

3.4.4 Advanced: On-Module FEATURES Options Summary Battery Disabled Optimal Default, Failsafe Default Management One Battery Enabled to support battery in ACPI OS by I2C_CK, I2C_DAT (B33,B34) Chapter 3 – AMI BIOS Setup...

[Page 42: Advanced: Sio Configuration](#)

3.4.5 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

[Page 43: Sio Configuration: Serial Port 9 Configuration](#)

3.4.5.1 SIO Configuration: Serial Port 9 Configuration Options Summary Use This Device Disabled Enabled Optimal Default, Failsafe Default Enabled or Disabled this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2D8h; IRQ=11; DMA ;

IO=2C8h;...

[Page 44: Sio Configuration: Serial Port 10 Configuration](#)

3.4.5.2 SIO Configuration: Serial Port 10 Configuration Options Summary Use This Device Disabled Enabled Optimal Default, Failsafe Default Enabled or Disabled this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2C8h; IRQ=10; DMA ; IO=2D8h;...

[Page 45: Advanced: Power Management](#)

3.4.6 Advanced: Power Management Options Summary Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select system power mode. Restore AC Power Last State Loss Always On Always Off Optimal Default, Failsafe Default Wake on LAN Enabled Optimal Default, Failsafe Default Enable...

[Page 46: Advanced: Digital Io Port Configuration](#)

3.4.7 Advanced: Digital IO Port Configuration Options Summary GPI * Input Optimal Default, Failsafe Default Output Set DIO as Input or Output Interrupt Disabled Optimal Default, Failsafe Default Enabled Enabled interrupt function with low pulse mode. This triggered pulse needs more than the 10ms.

[Page 47: Advanced: On-Module Hardware Monitor](#)

3.4.8 Advanced: On-Module Hardware Monitor Chapter 3 – AMI BIOS Setup...

[Page 48: Fan 1 Mode Configuration: Cpu Smart Fan Full Mode](#)

3.4.8.1 Fan 1 Mode Configuration: CPU Smart Fan Full Mode Options Summary CPU Smart Fan Full Mode Optimal Default, Failsafe Default control Manual Mode by PWM Auto Mode by PWM PWM signal Non-inverting Optimal Default, Failsafe Default Inverting Select output PWM of inverting or non-uninverting signal Chapter 3 – ...

[Page 49: Fan 1 Mode Configuration: Cpu Smart Fan Manual Mode](#)

3.4.8.2 Fan 1 Mode Configuration: CPU Smart Fan Manual Mode Options Summary Manual Setting Optimal Default, Failsafe Default Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number: Chapter 3 – AMI BIOS Setup...

[Page 50: Fan 1 Mode Configuration: Cpu Smart Fan Auto Mode](#)

3.4.8.3 Fan 1 Mode Configuration: CPU Smart Fan Auto Mode Options Summary Monitor Thermal CPU Temperature(DTS) Optimal Default, Failsafe Default Thermal Source 1(T1) Thermal Source 2(T2) Select monitor thermal source Temperature of Start Optimal Default, Failsafe Default Temperature Of Start Temperature Of Off Optimal Default, Failsafe Default...

[Page 51: Advanced: Trusted Computing](#)

3.4.9 Advanced: Trusted Computing Options Summary Security Device Disable Support Enable Optimal Default, Failsafe Default Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

[Page 52](#) Options Summary Platform Hierarchy Disable Enable Optimal Default, Failsafe Default Enable or Disable Platform Hierarchy Storage Hierarchy Disable Enable Optimal Default, Failsafe Default Enable or Disable Storage Hierarchy Endorsement Disable Hierarchy Enable Optimal Default, Failsafe Default Enable or Disable Endorsement Hierarchy TPM 2.0 UEFI Spec TCG_2...

[Page 53: Advanced: Firmware Update Configuration](#)

3.4.10 Advanced: Firmware Update Configuration Options Summary Me FW Image Disable Optimal Default, Failsafe Default Re-Flash Enable Enable/ Disable Me FW Image Re-Flash function. Chapter 3 – AMI BIOS Setup...

[Page 54: Setup Submenu: Chipset](#)

3.5 Setup submenu: Chipset Chapter 3 – AMI BIOS Setup...

[Page 55: Chipset: System Agent \(Sa\) Configuration](#)

3.5.1 Chipset: System Agent (SA) Configuration Chapter 3 – AMI BIOS Setup...

[Page 56: System Agent \(Sa\): Graphics Configuration](#)

3.5.1.1 System Agent (SA): Graphics Configuration Options Summary Primary Display Auto Optimal Default, Failsafe Default IGFX Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx. Primary IGFX Boot VBIOS Default Optimal Default, Failsafe Default Display DDI1/DP...

[Page 57: Graphics Configuration: Lvds Panel Configuration](#)

3.5.1.2 Graphics Configuration: LVDS Panel Configuration Options Summary Panel Type 640x480@60Hz 800x480@60Hz 800x600@60Hz 1024x600@60Hz 1024x768@60Hz Optimal Default, Failsafe Default 1280x768@60Hz 1280x800@60Hz 1280x1024@60Hz 1366x768@60Hz 1440x900@60Hz 1600x1200@60Hz 1920x1080@60Hz 1920x1200@60Hz Select panel type Chapter 3 – AMI BIOS Setup...

[Page 58](#) Options Summary Color Depth 18-bit Optimal Default, Failsafe Default 24-bit Select Color Depth Backlight Type Normal Optimal Default, Failsafe Default Inverted Select backlight control signal type Backlight Level Optimal Default, Failsafe Default 100% Select backlight control level Backlight PWM Freq 100Hz 200Hz...

[Page 59: Chipset: Pch-Io Configuration](#)

3.5.2 Chipset: PCH-IO Configuration Options Summary HD Audio Disabled Enabled Auto Optimal Default, Failsafe Default Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled Auto = HDA will be enabled if present, disabled otherwise. PCH LAN Enabled Optimal Default, Failsafe Default...

[Page 60: Chipset: Pcie Type Switch Selection](#)

3.5.3 Chipset: PCIE Type Switch Selection Options Summary PCIe Controller1 PCIe Port0~3 are four X1 Configuration PCIe Port0~3 is one X4 Optimal Default, Failsafe Default Select PCI Express Root Port * Selection. PCI Express Root Disabled Port 1 Enabled...

[Page 61: Setup Submenu: Security](#)

3.6 Setup submenu: Security Change Administrator/User Password You can set an Administrator password. If you set an Administrator password, you can then set a User password. User passwords do not have access to many of the features in the Setup utility.

[Page 62: Security: Secure Boot](#)

3.6.1 Security: Secure Boot Options Summary Attempt Secure Boot Disabled Optimal Default, Failsafe Default Enabled Secure Boot activated when Platform Key(PK) is enrolled, System mode is User/Deployed, and CSM function is disabled Secure Boot Mode Standard Custom Optimal Default, Failsafe Default Secure Boot Mode selector: Standard/Custom.

[Page 63: Secure Boot: Key Management](#)

3.6.1.1 Secure Boot: Key Management Options Summary Provision Factory Disabled Optimal Default, Failsafe Default Defaults Enabled Allow to provision factory default Secure Boot keys when System is in setup Mode Install Factory Default keys Force System to User Mode - install all Factory Default keys Enroll Efi Image Allow the image to run in Secure Boot mode.

[Page 64](#) Options Summary Platform Key(PK) Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test Key Exchange Keys Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)

[Page 65](#) Options Summary Forbidden Signatures Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test Authorized TimeStamps Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in:

a)EFI_SIGNATURE_LIST...

[Page 66: Setup Submenu: Boot](#)

3.7 Setup submenu: Boot Options Summary Quiet Boot Disabled Enabled Optimal Default, Failsafe Default Enables or Disables Quiet Boot option. Launch PXE Boot Disabled Optimal Default, Failsafe Default UEFI Legacy Controls the execution of UEFI and Legacy PXE OpROM. BIOS MODE UEFI and Legacy Optimal Default, Failsafe Default...

[Page 67: Boot: Hard Drive Bbs Priorities](#)

3.7.1 Boot: Hard Drive BBS Priorities Chapter 3 – AMI BIOS Setup...

[Page 68: Setup Submenu: Save & Exit](#)

3.8 Setup submenu: Save & Exit Chapter 3 – AMI BIOS Setup...

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Chapter 4 Chapter 4 – Drivers Installation...

[Page 70: Driver Download/Installation](#)

Driver Download/Installation Drivers for the COM-KBUC6/SKUC6 can be downloaded from the product page on the AAEON website by following this link:
<https://www.aaeon.com/en/p/com-express-modules-com-kbuc6> Download the driver(s) you need and follow the steps below to install them . 4.1 .1 COM-KBUC6 Driver Installation Steps Step 1 -...

[Page 71](#) Step 4 – Install Audio Driver Click the STEP4 - Audio folder followed by 0008-64bit_Win7_Win8_Win81_Win10_R281.exe Follow the instructions Drivers will be installed automatically Step 5 – Install ME Driver Click the STEP5 - ME folder followed by SetupME.exe 2.

[Page 72: Com-Skuc6 Driver Installation Steps](#)

4.1 .2 COM-SKUC6 Driver Installation Steps Step 1 – Install Chipset Driver Click the Step1 - Chipset folder followed by SetupChipset.exe Follow the instructions Drivers will be installed automatically Step 2 – Install Graphics Driver Click the Step2 - Graphic folder and select your OS Click the Setup.exe file in the folder Follow the instructions Drivers will be installed automatically...

[Page 73](#) Step 5 – Install USB 3.0 (Windows 7 only) Click the STEP5 - USB 3.0 folder followed by Win7 folder 2. Click Setup.exe 3. Follow the instructions 4. Drivers will be installed automatically Step 6 – Install ME Driver Click the STEP5 - ME folder followed by Windows folder.

[Page 74: Appendix A - Watchdog Timer Programming](#)

Appendix A Appendix A - Watchdog Timer Programming...

[Page 75: Watchdog Timer Initial Program](#)

Watchdog Timer Initial Program Table 1 : Embedded BRAM relative register table Default Value Note Index 0x284(Note1) BRAM Index Register Data 0x285(Note2) BRAM Data Register Logical Device Number 0xA8(Note3) Watchdog Logical Device Number Function and Device Number 0x00(Note4) Watchdog Function/Device Number...

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```
// Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex
//This parameter is represented from Note1 #define byte EcBRAMData //This parameter is
represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3
#define byte BRAMFnDataReg //This parameter is represented from Note4 #define void
EcBRAMWriteByte(byte Offset, byte Value);...
```

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```
Main VOID // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) //
(boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure :
AaeonWDTEnable // This procedure will enable the WDT counting. AaeonWDTEnable();
***** Appendix A
```

- Watchdog Timer Programming...

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// Procedure : AaeonWDTEnable AaeonWDTEnable () VOID WDTDisable(// Procedure :
AaeonWDTConfig AaeonWDTConfig () VOID // Disable WDT counting WDTDisable(// WDT
relative parameter setting WDTParameterSetting(); WDTDisable(byte Value) VOID
ECBRAMWriteByte(TimerReg , Value); WDTParameterSetting() VOID Byte TempByte; //
Watchdog Timer counter setting ECBRAMWriteByte(TimerReg , TimerVal);...

[Page 79](#) *****
ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value) VOID IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData,
0x30); //Write start ECBRAMReadByte(byte OPReg) Byte IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x12);
IOWriteByte(EcBRAMData, 0x10);...

[Page 80: Appendix B - I/O Information](#)

Appendix B Appendix B - I/O Information...

[Page 81: I/O Address Map](#)

I/O Address Map Appendix B - I/O Information...

[Page 82: Memory Address Map](#)

B.2 Memory Address Map Appendix B - I/O Information...

[Page 83: Irq Mapping Chart](#)

B.3 IRQ Mapping Chart Appendix B - I/O Information...

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[Page 93: Appendix C - Programming Digital I/O](#)

Appendix C Appendix C - Programming Digital I/O...

[Page 94: Digital I/O Programming](#)

Digital I/O Programming The COM-KBUC6 utilizes an AAEON chipset as its Digital I/O controller. Below are the procedures to complete its configuration, which you can use to develop a customized program to fit your application. C.2 Digital I/O Register Table 1 : Embedded BRAM relative register table Default Value Note...

[Page 95: Digital I/O Sample Program](#)

C.2 Digital I/O Sample Program

```
***** //  
Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex  
//This parameter is represented from Note1 #define byte EcBRAMData //This parameter is  
represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3  
#define byte BRAMFnData0Reg //This parameter is represented from Note4 #define byte  
BRAMFnData1Reg //This parameter is represented from Note5 #define void  
EcBRAMWriteByte(byte Offset, byte Value);...
```

[Page 96](#) *****

Main VOID Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read
Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin
level is High PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit); // Procedure :
AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...

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AaeonReadPinStatus(byte OptionReg, byte BitNum) Boolean Byte TempByte; TempByte =
ECBRAMReadByte(BRAMFnData1Reg, OptionReg); If (TempByte & BitNum == 0) Return 0;
Return 1; AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value) VOID Byte
TempByte; TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg); TempByte |= (Value
<< BitNum); ECBRAMWriteByte(OptionReg, BitNum, Value);...

[Page 98](#) *****

ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value) VOID IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData,
0x30); //Write start ECBRAMReadByte(byte FnDataReg, byte OPReg) Byte
IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg);
IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, FnDataReg);
IOWriteByte(EcBRAMIndex, 0x12);...

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Notes for Users Please observe the following items to ensure optimal performance: Always use
a new SSD with the latest firmware and SATA Gen3 cable for optimal performance and
compatibility. With the EHCI controller no longer available on the 6 Gen Intel Core™ ...

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