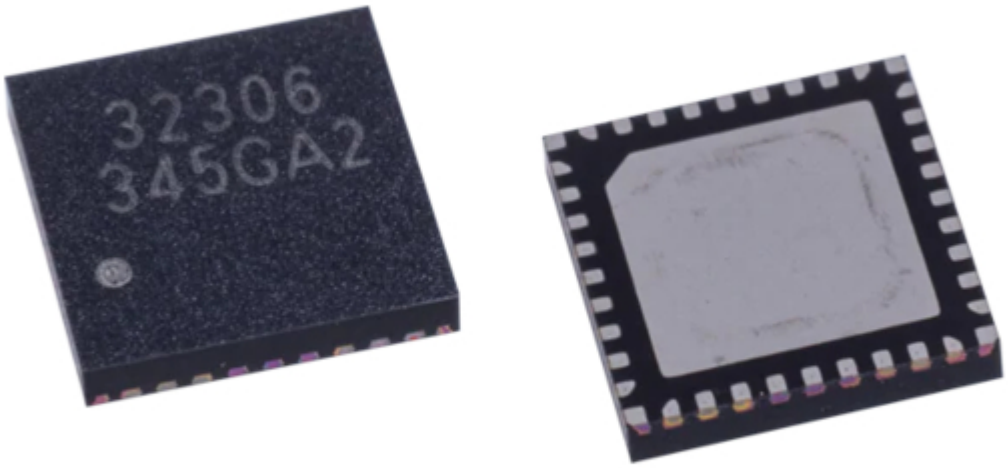
32306
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Toshiba TC32306FTG Manual

Single-chip rf transceiver for low-power systems

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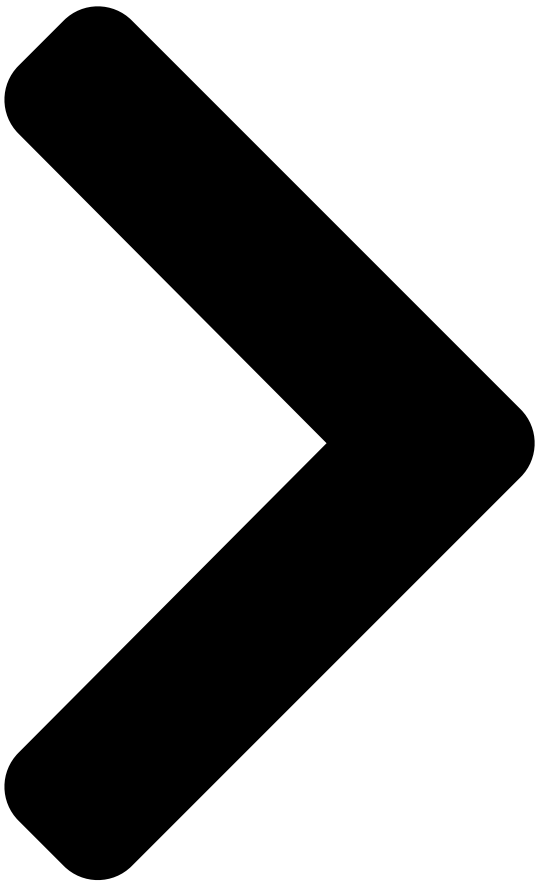


TOSHIBA

TC32306FTG

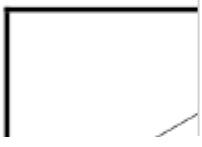
Single-Chip RF Transceiver for Low-Power Systems

1. General Description

The TC32306FTG is a single-chip RF transceiver, which provides many of the functions required for UHF-band transceiver applications. It has the most features transmitting and receiving the signal.

Furthermore, by digital processing, it can reduce significantly the number of external components and allow fine adjustments.

Various type of applications are supported by this chip as



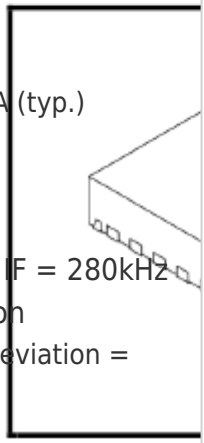
configuring various settings such as supply voltage, frequency, modulation and detection.

2. Applications

Remote keyless entry (remote door lock / unlock of equipment),
automotive equipment applications such as tire pressure monitoring system, and remote controller, etc

3. Features

• Integrates LNA, Mixer, IF Filter, IF AMP, RSSI, Signal Detector, Bit Rate Filter, Data Comparator, PLL, VCO
and PA into a single IC.



• Operating voltage range: 2.0 to 3.3 V (For 3V Use), 2.4V to 5.5V (For 5V Use)
• Current consumption: TX 12 mA at +10dBm output level / RX 9.7 mA / Battery Saving 0μA (typ.)
• Use for four RF Band: 315, 434, 868 / 915 MHz
• Supported modulation: ASK / FSK
• Single conversion system
• Two IF Filter bandwidth: wide 320kHz(typ.) at IF = 230kHz / middle 270kHz(typ.) at IF = 280kHz
• Signal Detections: RSSI detection, Noise detection (Only for FSK), Preamble detection
• Receiver sensitivity: under -116dBm (At IF BW = 320kHz, data rate = 600Hz, frequency deviation = +/-40kHz)
• Transmitter power: +10dBm (typ. at setting maximum output)
• Serial control (4 wire SPI) / EEPROM control
• Data Comparator Quick Charge / AutoOff Control / Antenna Switch Control

TOSHIBA CMOS Integrated Circuit Silicon Monolithic

1

TC32306FTG

QFN36-P-0606-0.50
Weight: 0.08 g (typ.)

2015-10-01

Next Page

Related Manuals for Toshiba TC32306FTG

Transceiver Toshiba NetPac Installation And Operation Manual

Wireless system (27 pages)

Transceiver Toshiba ZS-7222A Service Data

2w (22 pages)

Summary of Contents for Toshiba TC32306FTG

Page 1 TOSHIBA CMOS Integrated Circuit Silicon Monolithic TC32306FTG Single-Chip RF Transceiver for Low-Power Systems General Description The TC32306FTG is a single-chip RF transceiver, which provides many of the functions required for UHF-band transceiver applications. It has the most features transmitting and receiving the signal.

Page 2 TC32306FTG Block Diagram D_REG PA_GND2 XOSC Reference clock PA_OUT PA_GND1 Divider Data MOSI IF_REF COMP IF AMP MISO A_GND IF Filter Detector COM_VDD A_REG Limiter DET_TMONI1 A_VDD_3V RSSI RF_OUT DATA_IO Monitor IO_GND A_VDD_5V Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Page 3 TC32306FTG Pin Description 5.1 Equivalent Circuit and Function Table 5-1 Pin Description - All the values (resistance, capacity, etc.) shown in the internal equivalent circuit diagram are typical values. - The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purpose.

Page 4 TC32306FTG Pin No. Pin Name Description Internal Equivalent Circuit RSSI Output A_VDD_3V A_VDD_3V Output RSSI (= Received Signal Strength Indication) voltage. Connect ground via a capacitor. This IC has another RSSI signal for digital processing. Analog At no use, connect ground via a capacitor.

Page 5 TC32306FTG Pin No. Pin Name Description Internal Equivalent Circuit Analog 5V Supply Supply to mainly analog block. A_VDD_5V - For 5V use, supply 5V (typ.). - For 3V use, connect A_VDD_3V pin and supply 3V (typ.). RF Output pin RF_OUT RF signal output from LNA block, Open drain output.

Page 6 EEPROM Mode, EEPROM User Test Digital MODE2 Input Mode. Mode Control MODE1 Select SPI Mode, SPI User Test Mode, EEPROM Mode, EEPROM User Test Digital MODE1 Mode. Input 40kΩ TEST TEST Only use for Toshiba test. Connect ground. Digital TEST Input 40kΩ 2015-10-01...

Page 7 TC32306FTG Pin No. Pin Name Description Internal Equivalent Circuit Regulator Output for PLL COM_VDD COM_VDD Supply to mainly PLL block. Connect a Vref bypass capacitor. □ □ Do not supply voltage, and do not supply to an external circuit. PLL_REG...

Page 8 TC32306FTG Pin No. Pin Name Description Internal Equivalent Circuit Chip Select Input Control In SPI Mode / SPI User Test Mode / EEPROM User Test Mode. COM_VDD Digital Notice: Input Do not supply higher voltage than the level COM_VDD of COM_VDD. (For example, in the case of too low / no power supply.) That causes...

Page 9 Digital DET_TMONI1 Output At no use, open this pin. Control Data Output Demodulated signal output at RF-Receiving. Behavior of this pin is different for each state of TC32306FTG reset. See Table 5-2. Control COM_VDD Digital Notice: Output Output resistance of this pin is 10kΩ when the output drive setting is "Low".

Page 10 DET_TMONI3,4 Z: High Impedance Notice: In SPI Mode, TC32306FTG accepts the input of SPI settings at RESET = "L", but will not act. In Battery Saving Status, DATA_IO pin behavior changes to the value of register:h'0A[D5]RX_TX. Initial value of register:h’0A[D5]RX_TX

is “0”.

Page 11 6.1 Voltage Supply Settings The voltage supply of TC32306FTG is selectable either 3V or 5V. The supply voltage is selected by setting of 3V/5V pin, and it decides pin connections. At 5V use, connect 3V/5V pin to a voltage supply, then the internal voltage regulator (A_REG30;...

Page 12 6.1.3 Supply / Ground Connections In TC32306FTG supply / ground connections are separated for each functional block. At 5V use, some of analog functional blocks are connected internal 3V regulator (A_REG30 regulator). At 3V use, some of analog functional blocks are connected directly 3V supply, by connecting A_VDD_3V / A_VDD_5V pin.

Page 13 EEPROM Mode Setting and Connection EEPROM and MCU, connect via TC32306FTG. This IC is controlled by the register data of EEPROM. Select up to 8 configuration that are made as registers from “h'0A” to “h'1C”, depending on the size of EEPROM.

Page 14 6.3.1 Reset Status The internal condition (such as the register value) of TC32306FTG is initialized in this Status. For this IC Reset, input "L" signal to RESET pin surely during stable voltage supply. Also releasing Reset of this IC should be operated during stable voltage supply.

Page 15 X: Don’t care In SPI Mode, MODE 1 pin is unrelated to the status control of TC32306FTG. Moving to Battery Saving by AutoOff function, registers“h'0A[D7] ENB, h'0A[D6] ACT” keep the value “1”.

Page 16 It is a function to control external antenna switch. Set registers“h'0A[D3]TX_SW, h'0A[D2]RX_SW”, and TC32306FTG outputs control signals from TX_SW / RX_SW pin. The controls become valid at Run and Standby Status. These pins cannot be available in EEPROM Mode and EEPROM User Test Mode as using for input pins.

Page 17 Run / Standby PLL_LD X: Don’t care DET_out Signal TC32306FTG outputs the result of overall ”Detection” judgment depending on RSSI detection, Noise detection and/or Preamble detection. L: NOT determine ”Signal Detection” H: Determine ”Signal Detection” Set register:h'10[D2]DET_out_cnt_en=”1”, TC32306FTG holds DET_out output level "H" after first ”Signal Detection”.

Page 18 L: Battery Saving H: Standby / Run Un_DET_out Signal TC32306FTG outputs the result of overall ”No Signal Detection” judgment depending on RSSI detection , Noise detection and/or Preamble detection. L: NOT determine ”No Signal Detection” H: Determine ”No Signal Detection”...

Page 19 6.4.2 Reference Clock Prepare 30.32MHz reference clock for TC32306FTG. To use crystal oscillator, connect it between X_IN pin and X_OUT pin with load capacitors. This IC is designed and considered to connect a crystal oscillator with the load capacitance of 6pF.

Page 20 TC32306FTG PLL_LD signal from DET_TMONI1 pin and/or DET_TMONI2 pin, set registers“h'14[D6:D4], [D2:D0]”. Local Oscillation Setting for RX Set Local Oscillator frequency at "Lower Local". "Receiving Local Frequency" = "RF Recieving Frequency"–"IF Frequency" = "VCO Frequency" / "Division Ratio" Example 1 RF Frequency: 314.94MHz, IF Frequency: 280kHz, Division Ratio: 6 (Select 315MHz band)

Page 21 Fig 6-8 Receiver Block Diagram 6.5.2 Receiving Frequency Band TC32306FTG is available following frequency bands, 315, 434, and 868/915 MHz. 6.5.3 Receiver Gain Adjust overall gain of receiver block by matching network. The gain of LNA is controlled by the value of register: h'0E[D7:D6].

Page 22 6.5.4 IF Frequency TC32306FTG has the single conversion system. The output of LNA is downconverted to IF frequency by Image Cancel Mixer. Set IF frequency with adequate IF filter bandwidth by setting of register. Table 6-17 IF Frequency and Internal IF Filter Bandwidth...

Page 23 (h'0D[D0], h'0F[D0], h'12[D1:D0], h'13[D0], h'1A[D0], h'1B[D0], h'1C[D2:D0]), according to the Detection selections (Delay Detection; h'10[D0]Sel_Det = "0" / Pulse Count Detection; h'10[D0]Sel_Det = "1"). Table 6-20 is a recommended setting by Toshiba. Table 6-20 Settings of NIR Filter (Recommended Value)

Page 24 The cutoff frequency of LPF for FSK is about 20 kHz. Signal Detections In FSK, TC32306FTG is available 3 types of Signal Detections, RSSI Detection / Noise Detection / Preamble Detection. These Signal Detections have various sensitivity and accuracy, so select Signal Detection suitable to the application.

Page 25 Noise Detection monitors noise level near 34 kHz in FSK demodulation signal. Therefore, both “Signal Detection” and “No Signal Detection” in Noise Detection function may be false because of the noise reduction caused by high frequency signal. To avoid this, TC32306FTG has an additional function to improve detection accuracy.

Page 26 * tp: peak hold voltage charge coefficient, register:h’1C [D4:D3] Peak_Charge1..0 * tr: peak hold voltage discharge coefficient, register:h’1C [D7:D5] Peak_Ref2..0 When TC32306FTG starts to Run status, Peak Hold Circuit output voltage will reach 90% of the peak voltage during “tp’ / fbc x 2.30[s]”.

Page 27 Limiter will be bypassed when Data Comparator Quick Charge 2 is not used. Signal Detection In ASK, TC32306FTG is available 2 types of detections, RSSI Detection / Preamble Detection. Those detections are as same as that in FSK. Noise Detection cannot be available in ASK.

Page 28 Data Comparator Quick Charge 1 (During a certain period) The function is able to shorten the start period of TC32306FTG because time constant of vref will change to 1/16 or 1/4 only during that period. During start period, the output signal duty will be worse than that during normal condition, but Data Comparator output is obtained faster than the condition without Quick Charge 1.

Page 29 Notice: The register: h’0F[D3]Dataout_cnt_en is valid in RX. When the register: h’0F[D3] = “1”, TC32306FTG will output demodulated signal from the first rising edge of DET_out signal. Till the first rising edge of DET_out signal, this IC outputs “L”. When the register:h’0F[D3] = “1” and DET_out signal changes from “L” to “H”, this IC outputs demodulated signal in spite of the condition of DET_out signal till this IC will be Battery Saving or Standby mode.

Page 30 6.6.3 FSK Modulation To select FSK, set register:h’0A[D4] to “0”(FSK). TC32306FTG operates FSK modulation at PLL block with DATA_IO pin input signal. In FSK setting, the deviation is set by the register:h'12[D7:D2]Dev5..0. Available frequency deviation steps are different at each RF frequency band.

Page 31 6.6.4 ASK Modulation To select ASK, set register:h’0A[D4] to “1”(ASK). TC32306FTG operates ASK modulation by setting ON and OFF to RF-Transmitting Power Amplifier (PA) with DATA_IO pin input signal. If PA is enabled (See Table 6-33.), PA output is shown as table 6-32.

Page 32 TC32306FTG the signal holding state, set one of the follows. - Set TC32306FTG in the status of Battery Saving or Standby. - Change from TX to RX. - Change TX modulation. (ASK ↔ FSK) - Change RF frequency. (In the change in the value of register “h'0B” and/or “h'0C”) - Change the value of register:h’12[D7:D2] for TX deviation.

Page 33 MCU and TC32306FTG are connected by SPI lines and MCU controls this IC. MOSI MISO TC32306FTG Fig 6-13 Conceptual Connection of SPI Control In SPI Mode, TC32306FTG is available Single Read/Write and Burst Read/Write. These are selected from SPI instruction data. 2015-10-01...

Page 34 It is available for accessing to continuous address registers. To specify the start address only causes to shorten the read/write time. 6.7.3 SPI Control Data Format SPI control data format of TC32306FTG is constructed by instruction (8 bit), address (8 bit) and data (8 bit). Instruction Address...

Page 35 TC32306FTG 6.7.4 SPI Single Read/Write Write Set the single Read/Write (Write) data pattern to the instruction area. Set to register address to the next 8 bit, then register data to after next 8 bit. To write other address registers’ data continuously, repeat above routine.

Page 36 TC32306FTG 6.7.5 SPI Burst Read/Write Write This function continuously writes data to the order from the specified address. Set the burst Read/Write (Write) data pattern to the instruction area. Set to start register address to the next 8 bit, then register data to after next 8

bit. After that, repeat sequentially to set only 8 bit register data to the order.

Page 37 TC32306FTG Notice: After reading data reaches the last register address (h'FF), TC32306FTG continues to output data from the beginning address (h'00). During outputting register value from MISO pin, MOSI pin does not accept input data. To change the instruction or start register address, once set CS pin to be "H" in the Burst Read/Write.

Page 38 TC32306FTG 6.7.6 SPI Mode Signal Timings [Data Input Timing] CKWH CKWL MOSI High-Impedance MISO Fig 6-20 Example of SPI Write Timing [Data Output Timing] MOSI MISO Fig 6-21 Example of SPI Read Timing (Single Read/Write) [Data Output Timing]...

Page 39 6.7.7 EEPROM Mode EEPROM and MCU, connect via TC32306FTG. This IC is controlled by the register data of EEPROM. Select up to 8 configuration that are made as registers' modules from "h'0A" to "h'1C", depending on the size of EEPROM. In this mode, use of pins and external connections are different from those of SPI Mode.

Page 40 RESET pin from "L" to "H". TC32306FTG operates Burst Read to the first set data area of EEPROM through SPI lines. Burst Read operates from the start address till the end address of the configuration data sequentially. After the reading, this IC starts to Run as the configuration of first set data area.

Page 41 TC32306FTG Table 6-40 Relation between EEPROM and TC32306FTG Register Address Pin Name Read Config. EEPROM Address EEPROM Size Order RX_SW TX_SW ... Config.1 ... ... Config.2 ... ... Config.3 ... ... Config.4 ... ... Config.5 .....

Page 42 TC32306FTG 6.7.9 EEPROM Mode Signal Timings RESET CSWH CSWH * This IC repeats three times to read configuration data from the EEPROM for the majority logic. Fig 6-25 Example of EEPROM Control Timing RESET CKWH CKWL MOSI MSB OUT LSB OUT...

Page 43 This is a mode to monitor internal digital signal for design, development, manufacturing or shipping inspection. Set MODE1 pin to be "H" and/or the register: USER_TEST bit is "1" then TC32306FTG moves to User Test. In User Test, various internal signals for the adjustment are converted to analog and are output from DET_TMONI3 pin or DET_TMONI4 pin by the setting of register.

Page 44 TC32306FTG Table 6-43 Inner Signal Monitor (DET_TMONI3 Pin) h'10[D3] USER_TEST h'15[D6] h'15[D5] h'15[D4] Status Signal MONI3_SEL2 MONI3_SEL1 MONI3_SEL0 MODE1Pin Battery Saving "Z" Run / Standby 0 and L "L" Output Run / Standby 1 or H BRF_out Run / Standby...

Page 45 In EEPROM User Test Mode, the register can be set by SPI with connecting EEPROM. In EEPROM Mode, TC32306FTG as a master reads the register data in EEPROM through SPI lines. But in EEPROM User Test Mode, this IC as a slave accepts input from SPI lines. In the case, instructions in SPI format are different from those of SPI Mode.

Page 46 Clock Oscillator is over a certain level. Delay is selected by the register setting. Set it with considering Reference Clock oscillation stabilization time. The start timing of Delay is whichever later that output level of Reference Clock oscillator will be over a certain level or that TC32306FTG status will move to Run by the register settings.

Page 47 TC32306FTG The setup sequence and operation of internal function blocks will start after setting Delay time from the output level of Reference Clock Oscillator is over a certain level. Signal Detections (RSSI & Noise Detection) with operating cycle (Initial value: 1.35 ms) set by register will start after the internal setup (about 0.22 ms) is finished.

Page 48 TC32306FTG Power On, and reset is released after the voltage supply becomes stable. Set registers if necessary with Standby (ENB pin = "H", register:h'0A[D7]ENB = "1", register:h'0A[D6]ACT = "0"). Then internal regulators and Reference Clock Oscillator start to operate. After the registers settings, set register:h'0A and move to Run.

Page 49 TC32306FTG Notice: To shorten the boot sequence of this IC, there is other way to be able to moving to Run without going through Standby. In this method, firstly set ENB pin = "H", h'0A [D7] ENB = "1" and h'0A [D6] ACT = "1", then set other registers.

Page 50 The example of the transition “RX à TX à RX” in SPI Mode is shown as Fig 6-32. At the end of RX, set the register: h’0A[D5]RX_TX = ”1” then TC32306FTG changes to TX. After finishing all register settings for TX and CS pin is set to ”H”, this IC starts the setup sequence and PLL lock-up, then this IC is operated with setting registers.

Page 51 A or Type B. AutoOff Type A (AutoOff by Signal Detections) TC32306FTG will move from Run to Battery Saving if the determination of “No Signal Detection” is indicated (Un_DET_out signal = “H”). It is valid to set register:h'10[D5]AutoOffA_en = ”1”.

Page 52 - Continuing RX in AutoOff Type A When AutoOff Type A is valid, TC32306FTG will keep to be RX despite of the condition of Un_DET_out signal and DET_out signal, once after DET_out signal turns to be “H” before Un_DET_out signal turns to be “H”.

Page 53 - Continuing RX in AutoOff Type B When AutoOff Type B is valid, TC32306FTG will stop the timer countdown and continue to be RX if DET_out signal turns to be “H” before the end of timer period set by register. After that, this IC keeps to be RX despite of the condition of DET_out signal.

Page 54 TC32306FTG 6.10 Register Overview & Description Available register’s addresses in SPI Mode are "h’09-h’23", and these in EEPROM Mode are "h’0A-h’1C". Table 6-52 Available Register Addresses Address Type Name EEPROM Mode Code h'09 R / W Software Reset ○ h'0A...

Page 55 TC32306FTG Table 6-53 View of Register Settings (Reset & Status Control) Register Settings Address Software Reset h'09[D7:D0] Reset Output Current Drive Setting h'0D[D3:D1] Status Control 1 h'0A[D7] Buttery Saving Reset is Released Status Control 2 h'0A[D6] Run / Standby Standby à...

Page 56 TC32306FTG Table 6-54 View of Register Settings (In Run Status) Register Settings Address Antenna Switch Control h'0A[D3:D2] Monitors h'14[D6:D4], h'14[D2:D0] Except DET_out Signal DET_out Signal DET_out Signal Output Control h'10[D2] User Test h'10[D3] Normal User Test Monitor Signal Output h'15[D6:D4], h'15[D2:D0]...

Page 57 TC32306FTG Table 6-55 View of Register Settings (Detections Overall) Register Settings Address Demodulation (FSK / ASK) h'0A[D4] NIR (Near Interference Rejection) Filter Enable / Disable h'10[D1] Disable NIR Filter Frequency Control h'1B[D2:D1] Enable h'0D[D0], h'0F[D0], h'12[D1:D0], h'13[D0], Threshold Level of Detection...

Page 58 - Others: Not Initialize After entering register:[D0] data, TC32306FTG becomes Reset status, and then the reset is released whichever faster the rising edge of next SPI-Clock signal or the rising edge of next SPI-CS signal. Set this IC to SPI Read, this IC outputs register’s data "b'00000000".

Page 59 TC32306FTG 6.10.3 h’0B VCO Frequency Settings 1 Table 6-58 Register (h’0B) Name FC11 FC10 Initial Type [D7:D4]NC3..0 [Local Frequency: Integer Counter] NC = 2 ×NC3+2 ×NC2+2 ×NC1+2 ×NC0 Initial Value: NC = 9 h’0C [D7:D0]FC7..0 & h’0B [D3:D0]FC11..8 [Local Frequency: Fractional Counter] FC = -2 ×FC11+2...

Page 60 TC32306FTG <Case of setting ftx = 433.92MHz> ftx = 433.92MHz / fosc = 30.32MHz / fstep = 10kHz (= 3032 / 30.32MHz) In this case, nd = 4, as frequency band is 433MHz, and the result of calculations aren't affected by f_if.

Page 61 Notice: To start TC32306FTG with this delay time, changing the status from Battery Saving / Standby to Run after setting this register. If this register is set during Run, this register setting will be valid after the next transition from Battery Saving / Standby to Run.

Page 62 The function is resumed automatically at the rising edge of CS signal after setting this register. TC32306FTG always outputs previous input value of the register whichever the auto resume or not, (If this register is written to "0", the register outputs "0", after that auto resume.)

Page 63 TC32306FTG [D0] NIR_L2 When to use NIR filter (h'10[D1]NIR_Fil_en = "1") and Delay Detection (h'10[D0]Sel_Det = "0"), set this register "1". When to use NIR filter (h'10[D1]NIR_Fil_en = "1") and Pulse Count Detection (h'10[D0]Sel_Det = "1"), set this register

"0".

Page 64 TC32306FTG 6.10.9 h’11 Charge2 Threshold Setting Table 6-64 Register (h’11) Name Charge2_ Charge2_ Charge2_ Charge2_ Charge2_ Charge2_ Charge2_ Charge2_ Initial Type [D7:D0]Charge2_Th7..0 [Quick Charge 2 Threshold Level] When to set Data Comparator Quick Charge 2 (h'10[D6]Charge2_en = “1”) and FSK Demodulation (h'0A[D4]FSK_ASK = "0"), this setting is valid.

Page 65 TX and the Internal LD Signal cannot be monitored. To release the signal holding state, set one of the follows. - Set TC32306FTG in the status of Battery Saving or Standby. - Change from TX to RX.

Page 66 Preamble_DET_ The result of Preamble detection RSSI_DET_out The result of RSSI detection NDET_out The result of Noise detection TC32306FTG status (Standby, Run) / Battery Status_MONI Saving Un_DET_out The result of ”No Signal Detection” PLL_LD The result of PLL lock detection [D3] Set to “0”...

Page 67 TC32306FTG 6.10.13 h’15 Monitor Settings2 Table 6-68 Register (h’15) Name MONI3_ MONI3_ MONI3_ MONI4_ MONI4_ MONI4_ SEL2 SEL1 SEL0 SEL2 SEL1 SEL0 Initial Type [D7] Set to “0” surely. [D6:D4]MONI3_SEL2..0 [DET_TMONI3 Pin Output] When to select User Test (h'10[D3]USER_TEST = "1" and/or MODE1 pin = ”H”), these settings are valid.

Page 68 TC32306FTG 6.10.14 h’16 RSSI Threshold Setting Table 6-69 Register (h’16) Name DRSSI_Th7 DRSSI_Th6 DRSSI_Th5 DRSSI_Th4 DRSSI_Th3 DRSSI_Th2 DRSSI_Th1 DRSSI_Th0 Initial Type [D7:D0]DRSSI_Th7..0 [RSSI Threshold Level of Detection] - Setting Range [D7:D0] = 0 - 255 (b’00000000 - b’11111111) Initial Value: 0 To set RSSI threshold level of detection, refer the value of “h’22[D7:D0] RSSI Level Monitor”.

Page 69 TC32306FTG [D6:D0]Err_Margin6..0 [Error Margin] When to set Preamble detection (h’0F[D6]Preamble_en = ”1”), this setting is valid. - Setting Range [D6:D0] = 0 - 127 (b’0000000 - b’1111111) Initial Value: 5 (b’0000101) See section 6.5.6 about the Function of Preamble Detection.

Page 70 To be valid the setting of this register setting, finish writing the value to this register before the internal setup will start. When the internal setup has finished and TC32306FTG is Run status, move this IC status to Battery Saving / Standby and change this register value.

Page 71 TC32306FTG [D4:D3]Pre_DetCount1..0 [Preamble Detection Number of Times for Judgment] - Judged "Detection" by continuous detection within the error margin. - Judged "No Detection" by continuous detection outside the error margin. [D2]Pre_DetTrig [Preamble Detection Trigger] 0: Judged by period (Checked at the rising edge of the signal)

Page 72 TC32306FTG [D7:D6]Charge2_Ref1..0 [Data Comparator Quick Charge Coefficient] When to set Data Comparator Quick Charge 2 (h'10[D6]Charge2_en = “1”), this setting is valid. Set the tracking time constant τ of the data comparator reference voltage (vref). This is valid only if an absolute value of the difference between vref and vi (Data comparator input voltage) will be greater than the threshold level set by register:h’11[D7:D0]Charge2_Th7..0”.

Page 73 TC32306FTG 6.10.20 h’1C Peak Hold Settings Table 6-75 Register (h’1C) Name Peak_ Peak_ Peak_Ref2 Peak_Ref1 Peak_Ref0 NIR_2L0 NIR_L1 NIR_L0 Charge1 Charge0 Initial Type [D7:D5] Peak_Ref2..0 [Limiter (Peak Hold Voltage Discharge Coefficient)] When to set ASK Demodulation (h'0A[D4]FSK_ASK = "1") and Data Comparator Quick Charge 2 (h’10[D6]Charge2_en = ”1”), this setting is valid.

Page 74 When to set AutoOff Type B (h'10[D4]AutoOffB_en = “1”), this setting is valid. Set value of timer period till the function of AutoOff Type B starts to operate. TC32306FTG will move to Battery Saving after the value of timer period is passed, if this IC will not find "Signal Detection" after the boot sequence.

Page 75 TC32306FTG [D5]Noise_DET [Noise Detection] 0: During the detection / Disable 1: Detected (NDET_out Signal = ”H”) [D4]Pre_DET [Preamble Detection] 0: During the detection / Disable 1: Detected (Preamble_DET_out Signal = ”H”) [D3:D0] This output is always “0”. 6.10.23 h’1F Peak Hold Level Monitor Table 6-78 Register (h’1F)

Page 76 TC32306FTG 6.10.26 h’22 RSSI Level Monitor Table 6-81 Register (h’22) Name DRSSI7 DRSSI6 DRSSI5 DRSSI4 DRSSI3 DRSSI2 DRSSI1 DRSSI0 Type [D7:D0]DRSSI7..0 [Digital RSSI Level Monitor] The output is 8 bit Digital RSSI level. When Digital RSSI circuit is disabled, the output of this register is the value "b'00000000".

Page 77 TC32306FTG Absolute Maximum Ratings Table 7-1 Absolute Maximum Ratings (The temperature for unspecified temperature ranges is Ta = 25°C; voltage is ground referenced.) Characteristics Symbol / Pin Name Rating Unit Power supply voltage 1 COM_VDD, A_VDD_5V Min. -0.2 / Max. +6.0...

Page 78 TC32306FTG Operating Range Table 8-1 Operating Range (The temperature for unspecified temperature ranges is Ta = 25°C; voltage is ground referenced.) Test Characteristics Symbol Test Condition Typ. Unit Circuit Temperature range Topr °C Supply voltage range DD (5V) (For 5V Use, in SPI Mode)

Page 79 TC32306FTG Table 9-2 Pin Characteristics Test Characteristics Symbol Test Condition Typ. Unit Circuit COM_VDD Input low voltage 1 -0.2 × 0.2 Leakage current 1 µA (Low voltage input) ENB, RESET, 3V/5V, MODE2, DATA_IO, MISO, MOSI, CLK, CS COM_VDD COM_VDD Input high voltage 1 COM_VDD ×...

Page 80 TC32306FTG Table 9-3 RF-Receiving Characteristics Test Characteristics Symbol Test Condition Typ. Unit Circuit 50 Ω termination LNA gain 11-4 v (LNA) fo-3dB point IF filter lower cutoff frequency 1 IF = 230kHz / Wide band fo-3dB point IF filter higher cutoff frequency 1...

Page 81 TC32306FTG 10. Reference Characteristics Data This item contains reference values and does not contain any guaranteed values. (Unless otherwise specified, Ta = 25°C, VDD = 5.0V (For 5V use), fin(RF) = 314.94MHz, fin(X_IN) = 30.32MHz, Vin(X_IN) = 1.5Vp-p, deviation = +/-40kHz, fmod = 600Hz, FSK modulation, ENB = High, f(IF) = 230kHz(Wide band), Set register:h’0A[D7] = “1”, Set other registers initial)

Page 82 TC32306FTG (Unless otherwise specified, Ta = 25°C, V = 5.0V (For 5V use), fin(RF) = 314.94MHz, fin(X_IN) = 30.32MHz, Vin(X_IN) = 1.5Vp-p, FSK modulation, ENB = High, RF transmitting, Unmodulated, Set register:h’0A[D7] = “1”, Set other registers initial) Table 10-3 Reference RF-Transmitting Characteristics Data...

Page 83 RF (868), RF (915) Notice: Measure after the parts tuning that shows a part number. TC32306FTG supply voltage is selected by SW1 and SW2. SW3 and SW4 allow selecting the crystal oscillator and external signal. Fig 11-1 Typical Test Circuit...

Page 84 = Vin / I RSSI Test Characteristics: R RSSI Vin(=0.2V) * It will be measured at no voltage supply to TC32306FTG, and applied lower voltage not to work internal protection diodes. Fig 11-3 Test Circuit (RSSI_OUT Pin Output Resistance) 2015-10-01...

Page 85 TC32306FTG 50 Line 50 Line Measuring Signal Iinstrument Measuring Source Instrument (a) Measuring Instrument (b) 50 Line Signal Source Test Characteristics: DR RSSI1, RSSI2, RSSI3 * Measure DRfm by connecting (a). Test Characteristics: G Measure V by connecting (b). v (LNA)

Page 86 TC32306FTG 12. Reference data (This is temperature characteristics data when it used test circuit boards. This is not guarantee on condition that it is stating except electrical characteristics.) FSK Current Consumption vs. RX Current Consumption vs. Power Supply Voltage Characteristics Power Supply Voltage Characteristics 314.94MHz...

Page 87 TC32306FTG ASK Current Consumption vs. MIX Intercept Point Power Supply Voltage Characteristics 314.94MHz VDD=3.0V (3V use) IIP3: -9dBm 115°C 1dB comp (Input): -18dBm 25°C -40°C Desired wave <Desired> f(RF)in=314.94MHz VDD: 5V use <Un-desired> f(RF)in=314.94MHz f(RF)in=313.94MHz ASK mode Un-desired wave +312.94MHz...

Page 88 TC32306FTG S-Curve Characteristics (Pulse count detection) S-Curve Characteristics (Delay detection) -70dBm -50dBm -90dBm -90dBm -70dBm -100dBm -100dBm -50dBm -110dBm -110dBm -120dBm -120dBm VDD=3.0V (3V use) VDD=3.0V (3V use) f(RF)in=314.94MHz f(RF)in=314.94MHz FSK, delay detection FSK, pulse count detection <Meas

point> <Meas point>...

Page 89 TC32306FTG Duty Ratio vs. Power Supply Voltage Duty Ratio vs. Power Supply Voltage Characteristics (5V use) Characteristics (3V use) 3V use f(RF)in=314.94MHz V(RF)in=-50dBm fmod=600Hz FSK: +/-40kHz ASK: 90% depth <Meas point> DATA_IO at oscilloscope 5V use f(RF)in=314.94MHz V(RF)in=-50dBm fmod=600Hz FSK: +/-40kHz ASK: 90% depth <Meas point>...

Page 90 TC32306FTG TX Current Consumption vs. TX Current Consumption vs. Power Supply Voltage Characteristics Power Supply Voltage Characteristics 314.94MHz 115°C 915MHz 433.92MHz -40°C 25°C 314.94MHz VDD: 5V use FSK mode VDD: 5V use f(RF)out=314.94MHz FSK mode PA: maximum output PA: maximum output <Meas point>...

Page 91 TC32306FTG PA Output Level Frequency Characteristics VDD=3.0V (3V use) FSK mode 315MHz operation PA: maximum output <Meas point> PA_OUT at spectrum analyzer RF output frequency (MHz) 2015-10-01...

Page 92 TC32306FTG 13. Application Circuits Toshiba does not guarantee this application circuit example as a production design. Please evaluate carefully when developing the production design for your application. 13.1 Example of Evaluation Circuit is an example of Toshiba’s evaluation circuit. Fig 13-1 Power ON RESET 30.32MHz...

Page 93 - In above circuit, a control of an antenna switch is not use. 12pF 10pF - The capacitor C5 and C6 is adjusted by a trimmer capacitor. Toshiba use capacitors shown in the following, Murata Manufacturing 27pF 20pF Company, Ltd.

Page 94 Fig 13-2 Example of Application Circuit 1 - Fig 13-2 is SPI Mode and external MCU I/O is connected to SPI control pins of TC32306FTG, - Fig 13-2 is 3V Use. For 5V Use, change the voltage supply connections by referring Fig 13-1.

Page 95 Fig 13-3 Example of Application Circuit 2 - Fig 13-3 is SPI Mode and external MCU I/O is connected to SPI control pins of TC32306FTG, - Fig 13-3 is 3V Use. For 5V Use, change the voltage supply connections by referring Fig 13-1.

Page 96 Fig 13-4 Example of Application Circuit 3 - Fig 13-4 is EEPROM Mode and external EEPROM I/O is connected to SPI control pins of TC32306FTG, - Fig 13-4 is 5V Use. For 3V Use, change the voltage supply connections by referring Fig 13-1.

Page 97 Fig 13-5 Example of Application Circuit 4 - Fig 13-5 is the EEPROM Mode and external EEPROM I/O is connected to SPI control pins of TC32306FTG, - Fig 13-5 is 5V Use. For 3V Use, change the voltage supply connections by referring Fig 13-1.

Page 98 Lot Code 1) The year of manufacture (1 last figure of the year) 2) The week of manufacture (“01” as first week of the year, from 1 to 52 or 53) 3) Toshiba factory management code 4) Assembly code 2015-10-01...

Page 99 TC32306FTG 15. Package Dimensions Unit:mm QFN36-P-0606-0.50 Weight: 0.08g (Typ.) 2015-10-01...

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Page 101 TC32306FTG ..... 45 TATUS RANSITION 6.9.1 Power On à Battery Saving à Run .....46 6.9.2 Transition in Run Status (RX à TX à RX) .....50 6.9.3 Run à Battery Saving ..... 51 6.9.4 AutoOff Function .....51 6.9.5 Change Settings during Run .....

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This manual is also suitable for:

Tc32306ftgelTc32306ftgeltrTc32306ftgeltr-ndTc32306ftgrx