



Asus AAEON BOXER-6403M User Manual

1

2

3

4

5

6

7

8

9

10

Table Of Contents

11

12

13

14

15

16

17

18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67

68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93

•

[Table of Contents](#)

•

Bookmarks

--

[Download this manual](#)

Quick Links



BOXER-6403M

Fanless Embedded Box PC

st

User's Manual 1

Ed

Last Updated: June 14, 2016



[Table of Contents](#)

[Next Page](#)

1
2
3
4
5

Related Manuals for Asus AAEON BOXER-6403M

[Industrial PC Asus Aaeon BOXER-6639M User Manual](#)

Fanless embedded box pc (104 pages)

[Desktop Asus AAEON RTC-1010M User Manual](#)

Semi-rugged tablet computer (55 pages)

[Desktop Asus AAEON RTC-700M User Manual](#)

Rugged tablet computer (58 pages)

[Desktop Asus Vintage AE1 Quick Start Manual](#)

Barebone system (80 pages)

[Desktop Asus AS-D692 User Manual](#)

As-d692 user's manual for traditional chinese edition (96 pages)

[Desktop Asus BM5265 User Manual](#)

User manual (30 pages)

[Desktop Asus AS-M5200 User Manual](#)

User manual (44 pages)

[Desktop Asus AS-M5100 User Manual](#)

User manual (40 pages)

[Desktop Asus BP5220 User Manual](#)

User manual (74 pages)

[Desktop Asus A31AD User Manual](#)

(62 pages)

[Desktop Asus K31ADE User Manual](#)

(64 pages)

[Desktop Asus K20CD User Manual](#)

(50 pages)

[Desktop Asus A4320 Series User Manual](#)

(76 pages)

[Desktop Asus Vivo AiO V220 Series User Manual](#)

(66 pages)

[Desktop Asus Vivo AiO V222F Series User Manual](#)

(58 pages)

[Desktop Asus K20CD-K User Manual](#)

(50 pages)

Summary of Contents for Asus AAEON BOXER-6403M

[Page 1](#) BOXER-6403M Fanless Embedded Box PC User's Manual 1 Last Updated: June 14, 2016...

[Page 2](#) Copyright Notice This document is copyrighted, 2016. All rights are reserved. The original manufacturer reserves the right to make improvements to the products described in this manual at any time without notice. No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means without the prior written permission of the original manufacturer.

[Page 3](#) Acknowledgement All other products' name or trademarks are properties of their

respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. □ Intel, Pentium, Celeron, and Xeon are registered trademarks of Intel Corporation □ Atom is a trademark of Intel Corporation □...

Page 4 Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity BOXER-6403M □ Burn-proof bracket □ RJ-45 to D-sub cable □ Power adapter □ Product DVD with User's Manual (in pdf) and drivers □...

Page 5 About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the AAEON.com for the latest version of this document.

Page 6 Safety Precautions Please read the following safety instructions carefully. It is advised you keep this manual for future references All cautions and warnings on the device should be noted. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale.

Page 7 As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers. If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii.

Page 8 FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Page 9 China RoHS Requirements (CN) 中国RoHS指令 AAEON Embedded Box PC/
Industrial System 中国RoHS指令 (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) 符合
中国RoHS指令要求

[Page 10](#) China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Embedded Box PC/ Industrial System Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) PCB &...

[Page 11: Table Of Contents](#)

Table of Contents Chapter 1 - Product Specifications1 Specifications2
Chapter 2 – Hardware Information4 Dimensions 5 List of Jumpers
.....7 2.2.1 AT/ATX Mode Selection (JP1)8 2.2.2 LVDS BKL Control Selection
(JP2)8 2.2.3 LVDS Power Selection (JP3)

[Page 12](#) 2.3.14 DDR3L SODIMM Slot (DIMM1) 20 2.3.15 Half Size MiniCard Slot (PCIE1) 20 2.3.16 PCI-E Full Size MiniCard Slot (PCIE2) 22 Installing HDD25
Chapter 3 - AMI BIOS Setup28 System Test and Initialization29 AMI BIOS Setup

Page 13 Product CD/DVD54 Appendix A - Watchdog Timer Programming56 Watchdog Timer Initial Program 57 Appendix B - I/O Information62 I/O Address Map63 Memory Address Map65 IRQ Mapping Chart66 Appendix C -...

[Page 14: Chapter 1 - Product Specifications](#)

Chapter 1 Chapter 1 - Product Specifications...

Page 15: Specifications

Specifications ® ® Intel Celeron /Atom Processor Processor □ DDR3L 1333 MHz SODIMM x 1, up to 8 GB System Memory □ Chipset □ □ Display HDMI HDMI x 1 Interface Others 18/24-bit single channel Onboard LVDS x 1 (internal) Storage CF-SATA □...

[Page 16](#) Audio KB/MS Others Lockable DC Jack x 1, HDMI x 1 Expansion PCIe ☐ ☐ MiniCard Full-size MiniCard w/ SIM slot x 1 Mini PCI ☐ Others Onboard USB Pin header x 1 Indicator Front ☐ Rear ☐ Power Requirement 12V DC in with lockable connector ☐...

[Page 17: Chapter 2 - Hardware Information](#)

Chapter 2 Chapter 2 – Hardware Information...

[Page 18: Dimensions](#)

Dimensions 158,00 95,00 Chapter 2 – Hardware Information...

[Page 19](#) V 0 1 2 G V 0 1 G 95,00 GW:1.5KG NW:0.8KG Chapter 2 – Hardware Information...

[Page 20: List Of Jumpers](#)

List of Jumpers Please refer to the table below for all of the system's jumpers that you can configure for your application Label Function AT/ATX Mode Selection LVDS BKLT Control Selection LVDS Power Selection LVDS BKLT Control Selection Clear CMOS Jumper Dry and Wet Contact Digital Input Power Selection Dry and Wet Contact Digital Output Power Selection Chapter 2 –...

[Page 21: At/Atx Mode Selection \(Jp1\)](#)

2.2.1 AT/ATX Mode Selection (JP1) 1 2 3 1 2 3 ATX Mode (Default) AT Mode 2.2.2 LVDS BKLT Control Selection (JP2) 1 2 3 1 2 3 VR Mode PWM Mode (Default) 2.2.3 LVDS Power Selection (JP3) 1 2 3 1 2 3 3.3 V (Default) 2.2.4 LVDS BKLT Power Selection (JP4)

[Page 22: Clear Cmos Jumper \(Jp5\)](#)

2.2.5 Clear CMOS Jumper (JP5) Normal (Default) Clear CMOS 2.2.6 Dry and Wet Contact Digital Input Power Selection (JP6) 1 2 3 1 2 3 Wet Contact Digital Input Dry Contact Digital Input (Default) 2.2.7 Dry and Wet Contact Digital Output Power Selection (JP7) 1 2 3 1 2 3 Wet Contact Digital Output...

[Page 23: List Of Connectors](#)

List of Connectors Please refer to the table below for all of the system's connectors that you can configure for your application Label Function HDMI Display USB 3.0 Connector COM2 RS-232/422/485 CN11 LPC Expansion I/F CN16 COM3 RS-232 I/F CN17 COM1 RS-232/422/485 CN22 BIOS SPI Flash Header...

[Page 24: Hdmi Display \(Cn1\)](#)

2.3.1 HDMI Display (CN1) Pin Name Signal Type Signal Level HDMI_TX2+ DIFF HDMI_TX2- DIFF HDMI_TX1+ DIFF HDMI_TX1- DIFF HDMI_TX0+ DIFF HDMI_TX0- DIFF HDMI_CLK+ DIFF HDMI_CLK- DIFF HDMI_DDC_CLK HDMI_DDC_DATA HDMI_PWR HDMI_HPD Chapter 2 – Hardware Information...

[Page 25: Usb 3.0 Connector \(Cn2\)](#)

2.3.2 USB 3.0 Connector (CN2) Pin Name Signal Type Signal Level USB_D- DIFF USB_D+ DIFF USB3.0 RX- DIFF USB3.0 RX+ DIFF USB3.0 TX- DIFF USB3.0 TX+ DIFF 2.3.3 COM2 RS-232/422/485 Connector (CN4) RS-232 RS-422 RS-485 DATA+ DATA- Chapter 2 – Hardware Information...

[Page 26: Lpc Expansion I/F \(Cn11\)](#)

2.3.4 LPC Expansion I/F (CN11) Pin Name Signal Type Signal Level LAD0 +3.3V LAD1 +3.3V LAD2 +3.3V LAD3 +3.3V +3.3V +3.3V LFRAME# LRESET# +3.3V LCLK LDRQ0 LDRQ1 SERIRQ +3.3V 2.3.5 COM3 RS-232 I/F (CN16) Chapter 2 – Hardware Information...

[Page 27: Com1 Rs-232/422/485 Connector \(Cn17\)](#)

RS-232 2.3.6 COM1 RS-232/422/485 Connector (CN17) RS-232 RS-422 RS-485 DATA+ DATA- Chapter 2 – Hardware Information...

[Page 28: Dry And Wet Contact Digital Input \(Cn23\)](#)

2.3.7 Dry and Wet Contact Digital Input (CN23) Chapter 2 – Hardware Information...

[Page 29](#) Dry Contact Wiring Wet Contact Wiring Digital input voltage range 10 ~ 25 V Pin Name Signal Type Signal Level Digital input 3 Input DRY (5V) WET (3~30V) Chapter 2 – Hardware Information...

[Page 30: Dry And Wet Contact Digital Output \(Cn24\)](#)

Digital input 2 Input DRY (5V) WET (3~30V) Digital input 1 Input DRY (5V) WET (3~30V) Digital input 0 Input DRY (5V) WET (3~30V) WET contact POWER 3~30V 2.3.8 Dry and Wet Contact Digital Output (CN24) Dry Contact Wiring Wet Contact Wiring User I/O Level Digital output voltage range 30 V...

[Page 31: Ethernet Port \(Cn26\)](#)

2.3.9 RJ-45 Ethernet Port (CN26) Pin Name Signal Type Signal Level MDI0+ DIFF MDI0- DIFF MDI1+ DIFF MDI2+ DIFF MDI2- DIFF MDI1- DIFF MDI3+ DIFF MDI3- DIFF 2.3.10 RJ-45 Ethernet Port (CN27) Pin Name Signal Type Signal Level MDI0+ DIFF MDI0- DIFF MDI1+...

[Page 32: Usb 2.0 Port 1 Connector \(Usb1\)](#)

MDI3+ DIFF MDI3- DIFF 2.3.11 USB 2.0 Port 1 Connector (USB1) Pin Name Signal Type Signal Level USB_D- DIFF USB_D+ DIFF 2.3.12 USB 2.0 Port 2 Connector (USB2) Pin Name Signal Type Signal Level USB_D- DIFF USB_D+ DIFF 2.3.13 USB 2.0 Port 3 Connector (USB3) Pin Name Signal Type Signal Level...

[Page 33: Ddr3L Sodimm Slot \(Dimm1\)](#)

2.3.14 DDR3L SODIMM Slot (DIMM1) Standard Specifications 2.3.15 Half Size MiniCard Slot (PCIE1) Pin Name Signal Type Signal Level +3.3V +3.3V +1.5V +1.5V Chapter 2 – Hardware Information...

[Page 34](#) mSATA RX+ DIFF +3.3V +3.3V mSATA RX- DIFF +1.5V +1.5V SMB_CLK +3.3V mSATA_TX DIFF SMB_DATA +3.3V mSATA_TX+ DIFF +3.3V +3.3V +3.3V +3.3V +1.5V +1.5V Chapter 2 – Hardware Information...

[Page 35: Pci-E Full Size Minicard Slot \(Pcie2\)](#)

+3.3V +3.3V 2.3.16 PCI-E Full Size MiniCard Slot (PCIE2) Pin Name Signal Type Signal Level +3.3V +3.3V +1.5V +1.5V Chapter 2 – Hardware Information...

[Page 36](#) PCIE RX- DIFF +3.3V +3.3V PCIE RX+ DIFF +1.5V +1.5V SMB_CLK +3.3V PCIE TX DIFF SMB_DATA PCIE TX+ DIFF +3.3V +3.3V +3.3V +3.3V Chapter 2 – Hardware Information...

[Page 37](#) +1.5V +1.5V +3.3V +3.3V Chapter 2 – Hardware Information...

[Page 38: Installing Hdd](#)

Installing HDD Remove the screws as shown below Note that connector side of the HDD should face the opposite side of the highlighted hole Chapter 2 – Hardware Information...

[Page 39](#) Secure the HDD with screws Attach the assembled HDD to the underside of the cover with screws Chapter 2 – Hardware Information...

[Page 40](#) Connect up the HDD using the cables as shown Chapter 2 – Hardware Information...

[Page 41: Chapter 3 - Ami Bios Setup](#)

Chapter 3 Chapter 3 - AMI BIOS Setup...

[Page 42: System Test And Initialization](#)

System Test and Initialization The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors. The system configuration verification routines check the current system configuration

against the values stored in the CMOS memory.

[Page 43: Ami Bios Setup](#)

AMI BIOS Setup The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off. To enter BIOS Setup, press ...

[Page 44: Setup Submenu: Main](#)

Setup Submenu: Main Chapter 3 – AMI BIOS Setup...

[Page 45: Setup Submenu: Advanced](#)

Setup Submenu: Advanced Chapter 3 – AMI BIOS Setup...

[Page 46: Advanced: Cpu Configuration](#)

3.4.1 Advanced: CPU Configuration Options summary: Intel Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default EIST Disabled Enabled Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 47: Advanced: Ide Configuration](#)

3.4.2 Advanced: IDE Configuration Options summary: SATA Mode IDE Mode AHCI Mode Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 48: Advanced: Usb Configuration](#)

3.4.3 Advanced: USB Configuration Options summary: Legacy USB Support Enabled Optimal Default, Failsafe Default Disabled Auto Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected Chapter 3 – ...

[Page 49: Advanced: Hardware Monitor](#)

3.4.4 Advanced: Hardware Monitor Chapter 3 – AMI BIOS Setup...

[Page 50: Advanced: Dynamic Digital Io Configuration](#)

3.4.5 Advanced: Dynamic Digital IO Configuration Options summary: GPO0 Direction [Output] Output Level Optimal Default, Failsafe Default GPO1 Direction [Output] Output Level Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 51: Advanced: Power Management](#)

3.4.6 Advanced: Power Management Options summary: Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select power supply mode. AC Power Loss Last State Optimal Default, Failsafe Default Power On Power Off Select power state when power is re-applied after a power failure. RTC wake system Disabled Optimal Default, Failsafe Default...

[Page 52: Advanced: Sio Configuration](#)

3.4.7 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

[Page 53: Sio Configuration: Serial Port 1 Configuration](#)

3.4.7.1 SIO Configuration: Serial Port 1 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=3F8; IRQ=4; IO=2F8; IRQ=3; Select an optimal setting for IO device Mode: RS232 Optimal Default, Failsafe Default...

[Page 54: Sio Configuration: Serial Port 2 Configuration](#)

3.4.7.2 SIO Configuration: Serial Port 2 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2F8; IRQ=3; IO=3F8; IRQ=4; Select an optimal setting for IO device Mode: RS232 Optimal Default, Failsafe Default...

[Page 55: Sio Configuration: Serial Port 3 Configuration](#)

3.4.7.3 SIO Configuration: Serial Port 3 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=3E8; IRQ=11; IO=2E8; IRQ=11; Select an optimal setting for IO device Chapter 3 –...

[Page 56: Setup Submenu: Chipset](#)

Setup submenu: Chipset Chapter 3 – AMI BIOS Setup...

[Page 57: Chipset: North Bridge](#)

3.5.1 Chipset: North Bridge Chapter 3 – AMI BIOS Setup...

[Page 58: Display Control Configuration](#)

3.5.1.1 Display Control Configuration Options summary: DVMT Pre-Allocated Optimal Default, Failsafe Default 128M 160M 192M 224M 256M 288M 320M 352M 384M 416M 448M 480M 512M DVMT Total Gfx Mem 128MB Chapter 3 – AMI BIOS Setup...

[Page 59](#) 256MB Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 60: South Bridge](#)

3.5.2 South Bridge Options summary: Audio Controller Disabled Enabled Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 61: Security](#)

Security Change User/Administrator Password You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility. Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers).

[Page 62](#) Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection. Chapter 3 – AMI BIOS Setup...

[Page 63: Setup Submenu: Boot](#)

Setup submenu: Boot Options summary: Quiet Boot Disabled Enabled Default En/Disable showing boot logo. Option ROM Messages Force BIOS Default Keep Current Set display mode for Option ROM Launch PXE OpROM Disabled Default Enabled En/Disable Legacy Boot Option Chapter 3 – AMI BIOS Setup...

[Page 64: Bbs Priorities](#)

3.7.1 BBS Priorities Chapter 3 – AMI BIOS Setup...

[Page 65: Setup Submenu: Exit](#)

Setup submenu: Exit Chapter 3 – AMI BIOS Setup...

[Page 66: Chapter 4 - Drivers Installation](#)

Chapter 4 Chapter 4 – Drivers Installation...

[Page 67: Product Cd/Dvd](#)

Product CD/DVD The BOXER-6403M comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers. In case the program does not start, follow the sequence below to install the drivers. Step 1 –...

[Page 68](#) Step 4 – Install xHCI Driver (Windows 7 only) Open the Step 4 - xHCI folder and followed by the Setup.exe file Follow the instructions Drivers will be installed automatically Step 5 – Install Intel Sideband Fabric Device Drivers (Windows 8.1 only) Open the Step 5 - Intel

Sideband Fabric Device followed by the Setup.exe file Follow the instructions...

[Page 69: Appendix A - Watchdog Timer Programming](#)

Appendix A Appendix A - Watchdog Timer Programming...

[Page 70: Watchdog Timer Initial Program](#)

A.1 Watchdog Timer Initial Program Table 1 : SuperIO relative register table Default Value Note
SIO MB PnP Mode Index Register Index 0x2E(Note1) 0x2E or 0x4E SIO MB PnP Mode Data
Register Data 0x2F(Note2) 0x2F or 0x4F Table 2 : Watchdog relative register table Register
BitNum Value...

[Page 71](#) *****
// SuperIO relative definition (Please reference to Table 1) #define byte SIOIndex //This
parameter is represented from Note1 #define byte SIOData //This parameter is represented
from Note2 #define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte
IOPort); // Watch Dog relative definition (Please reference to Table 2) #define byte TimerLDN
//This parameter is represented from Note3 #define byte TimerReg //This parameter is
represented from Note4 #define byte TimerVal // This parameter is represented from Note24...

[Page 72](#) *****
VOID Main(){ // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) //
(boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure :
AaeonWDTEnable // This procedure will enable the WDT counting. AaeonWDTEnable();
***** Appendix A
- Watchdog Timer Programming...

[Page 73](#) *****
// Procedure : AaeonWDTEnable VOID AaeonWDTEnable (){ WDTEnableDisable(EnableLDN,
EnableReg, EnableBit, 1); // Procedure : AaeonWDTConfig VOID AaeonWDTConfig (){ // Disable
WDT counting WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0); // Clear Watchdog
Timeout Status WDTClearTimeoutStatus(); // WDT relative parameter setting
WDTParameterSetting(); VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte
Value){ SIOBitSet(LDN, Register, BitNum, Value);...

[Page 74](#) *****
VOID SIOEnterMBPnPMode(){ IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); VOID
SIOExitMBPnPMode(){ IOWriteByte(SIOIndex, 0xAA); VOID SIOSelectLDN(byte LDN){
IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN);
VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){ Byte TmpValue;
SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue =
IOReadByte(SIOData);...

[Page 75: Appendix B - I/O Information](#)

Appendix B Appendix B - I/O Information...

[Page 76: I/O Address Map](#)

I/O Address Map Appendix B - I/O Information...

[Page 77](#) Appendix B - I/O Information...

[Page 78: Memory Address Map](#)

Memory Address Map Appendix B - I/O Information...

[Page 79: Irq Mapping Chart](#)

IRQ Mapping Chart Appendix B - I/O Information...

[Page 80](#) Appendix B - I/O Information...

[Page 81](#) Appendix B - I/O Information...

[Page 82](#) Appendix B – I/O Information...

[Page 83: Appendix C - Electrical Specifications For I/O Ports](#)

Appendix C Appendix C – Electrical Specifications for I/O Ports...

[Page 84: Electrical Specifications For I/O Ports](#)

Electrical Specifications for I/O Ports Reference Signal Name Rate Output Backlight +5V/0.5 or Brightness Control CN19 +VCC_LVDS_BKLT +12V/0.5 Connector Internal LVDS +3.3V/1A or CN25 Connector +5V/1A HDMI Connector +5V/1A +5V/1Aer USB3.0 Connector USB3 channel) +3.3VSB +3.3V/1.1A mSATA Connector PCIe1_A1 +1.5V +1.5V/0.375A COM1 +5V/0.5A or...

[Page 85: Appendix D - Digital I/O Ports](#)

Appendix D Appendix D – Digital I/O Ports...

[Page 86: Di/O Programming](#)

DI/O Programming The BOXER-6403M utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application. There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode (2) Modify the data of configuration registers (3) Exit the MB PnP Mode.

[Page 87: Digital I/O Register](#)

Digital I/O Register Table 2 : SuperIO relative register table Default Value Note SIO MB PnP Mode Index Register Index 0x2E 0x2E or 0x4E SIO MB PnP Mode Data Register Data 0x2F 0x2F or 0x4F Table 2 : Digital Input relative register table Register BitNum Value...

[Page 88: Digital I/O Sample Program](#)

Digital I/O Sample Program

```
***** // SuperIO
relative definition (Please reference to Table 1) #define byte SIOIndex //This parameter is
represented from Note1 #define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte IOPort); //
Digital Input Status relative definition (Please reference to Table 2) #define byte DInput1LDN //
This parameter is represented from Note3 #define byte DInput1Reg // This parameter is
represented from Note4...
```

[Page 89](#) *****

```
// Digital Output control relative definition (Please reference to Table 3) #define byte
DOutput1LDN // This parameter is represented from Note21 #define byte DOutput1Reg // This
parameter is represented from Note22 #define byte DOutput1Bit // This parameter is
represented from Note23 #define byte DOutput1Val // This parameter is represented from
Note24 #define byte DOutput2LDN // This parameter is represented from Note25 #define byte
DOutput2Reg // This parameter is represented from Note26...
```

[Page 90](#) *****

```
VOID Main(){ Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read
Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin
level is High PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit); //
Procedure : AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...
```

[Page 91](#) *****

```
Boolean AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){ Boolean PinStatus ;
PinStatus = SIOBitRead(LDN, Register, BitNum); Return PinStatus ; VOID
AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
ConfigToOutputMode(LDN, Register, BitNum); SIOBitSet(LDN, Register, BitNum, Value);
***** Appendix D
– Digital I/O Ports...
```

[Page 92](#) *****

```
VOID SIOEnterMBPnPMode(){ IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); VOID
SIOExitMBPnPMode(){ IOWriteByte(SIOIndex, 0xAA); VOID SIOSelectLDN(byte LDN){
IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN);
```

```
VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){ Byte TmpValue;  
SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue =  
IOReadByte(SIOData);...
```

[Page 93](#) *****

```
Boolean SIOBitRead(byte LDN, byte Register, byte BitNum){ Byte TmpValue;  
SIOEnterMBPnPMode(); SIOSelectLDN(LDN); IOWriteByte(SIOIndex, Register); TmpValue =  
IOReadByte(SIOData); TmpValue &= (1 << BitNum); SIOExitMBPnPMode(); If(TmpValue == 0)  
Return 0; Return 1; VOID ConfigToOutputMode(byte LDN, byte Register, byte BitNum){ Byte  
TmpValue, OutputEnableReg; OutputEnableReg = Register-1;...
```