Sanyo AVM-2550S Training Manual

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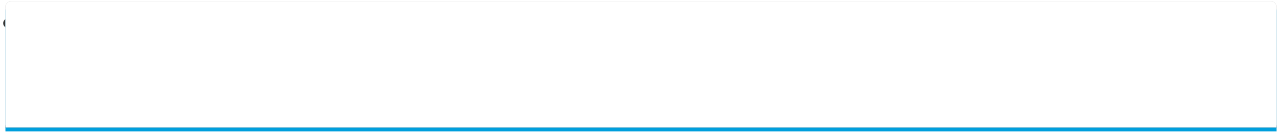

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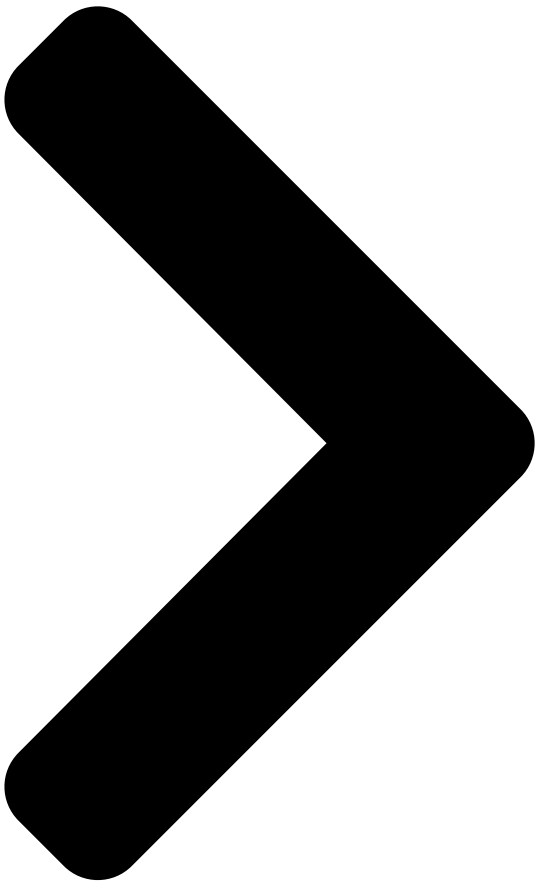

SANYO FISHER SERVICE CORPORATION

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TRAININ

INTRODUCTION TO THE VB7C CHASSIS (AVM-2780G)

TRAINING MANUAL

TI
REFERENCE No.
780010

INTRODUCTION TO THE VB7C CHASSIS (AVM-2780G)

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Related Manuals for Sanyo AVM-2550S

CRT TV Sanyo AVM-2550S, AVM-2759S Owner's Manual

Sanyo color tv owner's manual avm-2550s, avm-2759s (48 pages)

TV Sanyo AVM-3259S Owner's Manual

Color tv (56 pages)

CRT TV Sanyo AVM-2760S Owner's Manual

Sanyo avm-2760s: owners manual (48 pages)

Sanyo AVM-3259G Service Manual

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Color tv (40 pages)

TV Sanyo AVM-3650G Owner's Manual

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Summary of Contents for Sanyo AVM-2550S

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Page 2 Recommended Troubleshooting & Repairing Guide: V3.0 –LED & LCD TV V2.0- LCD TV Repair Repair Tips ebook Tips & Case Histories “More information on T-con Board & Mainboard Secret Repair Tips!” Vol-3 LCD/LED V1.0- Collection of LCD Monitor Repair Case TV Repair Tips Histories by Jestine Yong...

Page 3 C-003 CPU is used on all models using the VB7C chassis, which includes the procedures may result in damage or personal injury. AVM-2550S, AVM-2580G, AVM-2759S

(Chassis No. G5G-2759S2), AVM- 2760S, AVM-2780G, AVM-3259G (Chassis No. G5R-3259G2/3/4), AVM- Integrated circuits and many other semiconductors are electrostatically 3260G, AVM-3259S (Chassis No.

Page 4: Table Of Contents

TABLE OF CONTENTS AFT DEFEAT CIRCUIT • 32 INTRODUCTION TO THE C-003 CPU • • • • • • • • • • • • • • • 2 CPU PROGRAMMING •...

Page 5: Introduction To The C-003 Cpu

INTRODUCTION TO THE C-003 CPU The C-003 CPU tuning system is capable of electronically tuning 181 different 14. On-screen Service Adjustment Menu system channels and is similar to conventional synthesized tuning systems described 15. Automatic RF AGC adjustment system in earlier training manuals. The major difference between the C-003 and 16.

Page 6 COMPOSITE VIDEO PRE-AMP CAPTION DISPLAY DATA SLICER RF AGC BOARD A/D INPUT (C-003) BEAM CURRENT DETECTOR DIGICON SOUND EEPROM TUNER BUS CONTROLLED SIGNAL PROCESSOR PRE-SCALER BAND SW C-003 Tuning System Block Diagram – 3 –...

Page 7: Cpu Programming

CPU PROGRAMMING The On-screen Service Adjustment Menu system employed in the VB7C The Service Adjustment Menu display shown below and the following table chassis replaces the resistors used to change the voltage on the option pins show the different options available and the necessary data. The option data of the previous CPU.

Page 8 DATA FUNCTION –– –– NOT USED –– –– NOT USED –– –– NOT USED 00: NONE 3, 4 CLOCK 01: YES (AC 60 Hz) DATA 10: YES (INT OSC) XXX OPT XXXXXXXX 11: INHIBITED (=NONE) –– –– NOT USED SURROUND NONE BINARY DATA (8 bit) ––...

Page 9: Key Scan Circuit

KEY SCAN CIRCUIT Key Scan Key Input The Key Scan circuit uses an analog circuit to generate and send voltage to The function of the keys on keyboard and those of the remote control the CPU when a key is pressed. The CPU uses this voltage to determine transmitter are the same.

Page 10 IC801 ALWAYS R1910 R1902 R1903 R1904 R1905 R1906 R1907 R1901 L1901 SW1901 SW1902 SW1903 SW1904 SW1905 SW1906 (POWER) (VOL +) (VOL –) (MENU) D1901 C1902 (7.5V) Key Scan Circuit – 7 –...

Page 11: Remote Control Input

REMOTE CONTROL INPUT The data received from the remote control is first amplified to 5 V digital Custom and Data codes differentiate between the “1” and “9” values by the pulses by the pre-amplifier module A1901 and then input to the CPU on pin pulse duration.

Page 12 LEADER CODE CUSTOM CODE CUSTOM CODE DATA CODE DATA CODE C0 C1 C2 C3 C4 C5 C6 C7 D0 D1 D2 D3 D4 D5 D6 D7 4.5ms 27ms 27ms Remote Transfer Code 0.56ms 1.125ms 2.25ms 1.125ms 2.25ms " 0 " "...

Page 13: Pll Data Out Circuit

PLL DATA OUT CIRCUIT The VB7C chassis uses a new BUS-Controlled UHF/VHF Tuner with a built- Channel selection requires only two inputs from the CPU. These are the Data in Phase Locked Loop, Prescaler and Band Switch. Including these circuits signal input from pin 32, and the Clock signal input from pin 34.

Page 14 BYTE (MSB) DATA BYTE (LSB) COMMAND Address byte (ADB) MA1 MA0 Divider byte 1 (DB1) Divider byte 2 (DB2) Control byte (CB) Band switch byte (BB) FMT BVH BVL A • • • • • • • • • • • • • • • • acknowledge MA1 and MA2 •...

Page 15: Aft Circuit

AFT CIRCUIT The Automatic Fine Tuning (AFT) program incorporated in the CPU functions The Time Base signal is the AND signal of the horizontal sync signal from the to fine tune the tuner local oscillator to the center of the actual broadcast flyback transformer and the horizontal sync

signal from the video (Y) signal.

Page 16 3.3 V S-CURVE 1.67 V RANGE OF 0 ~ 5 V TIME BASE SIGNAL TUNING POINT AFT S-Curve Signal Station Center Time Base Signal – 13 –...

Page 17: Signal Processor Bus Control Circuit

SIGNAL PROCESSOR BUS CONTROL CIRCUIT The VB7C chassis is equipped with a new single-chip BUS-Controlled NTSC Control of the Signal Processor IC is through CPU pins 32 and 34. Signal Processor IC to replace much of the mechanically adjusted factory/service controls and all of the low pass filters in the PWM control lines Pin 34 is the BUS SCL (Serial Data) signal.

Page 18 IC Address: BAh (10111010) Register Name Bits General Description Sub Address (MSB) DATA (LSB) T Enable Disable the Test SW & enable Video Mute SW • • • • • • Video Mute Disable video outputs T_Enable Vid_Mute S Sync Kill Force free-run mode (tr0) ABL Defeat SW...

Page 19: Mts Processor Bus Control Circuits

MTS PROCESSOR BUS CONTROL CIRCUIT The VB7C chassis is equipped with a new single-chip BUS-Controlled MTS Control of the MTS Processor IC is through CPU pins 32 and 34. Processor IC to replace much of the mechanically adjusted factory/service controls and all of the low pass filters in the PWM control lines for the Pin 34 is the BUS SCL (Serial Clock) signal.

Page 20 IC Write Address: 84h (10000100) • Note-1: ATT for the Input Level Adjustment. • Note-2: SPECTRAL for the High Separation and WIDEBAND for Low Separation Sub Address (MSB) DATA (LSB) Adjustments. • • • • • • TEST-DA TEST 1 ATT (Note-1) •...

Page 21: Sound Control Circuit

SOUND CONTROL CIRCUIT The sound level is controlled by the BUS control signal form the CPU, the The volume control data “000000” and the audio mute control data “0” are BUS SDA (Serial Data) signal from pin 32, and the BUS SCL (Serial Clock) input to the Volume Control Registers VOL-L and VOL-R, and the Audio Mute signal from pin 34.

Page 22 IC3401 IC001 IC801 MTS PROCESSOR AUDIO AMP. C002 C010 R881 L881 R3401 SP901 VOL-R VOLUME SPEAKER (R) L882 R3402 R882 CONTROL VOL-L SP902 TREBLE SPEAKER (L) BASS/TREBLE C001 C011 CONTROL MUTE BASS Interface C007 R011 SURROUND to BUS Line SURR BLOCK Q001 FEXT1...

Page 23: Digital Control Circuits

DIGITAL CONTROL CIRCUITS Digital electronic controls replace the mechanical customer controls. This When the FACTORY PRESET mode is selected with the RESET key, the provides a more precise setting of the controls as well as allowing the Picture/Sound controls will return to the factory settings. During FACTORY convenience of remote operation.

Page 24 IC101 IC801 RANGE OF STEPS SIGNAL PROCESSOR OUTPUT FUNCTION RANGE OF CUSTOMER SERVICE BUS DATA L813 R803 Write Color CONTROL ADJUSTMENT 7 bit (0~64)/127x1.5 (0~31)/127 Write Tint Color 0 ~ 127 Interface 7 bit =0/127~96/127 =0/127~31/127 R804 L814 Write (0~64)/127x1.5 (0~31)/127 Contrast 7 bit...

Page 25: Power On/Off And Protection Circuits

POWER ON/OFF and PROTECTION CIRCUITS Power On/Off Note: The C-003 CPU provides a Power Surge Protection feature. If power The CPU performs the On/Off function through pin 27. In the Power On mode failures occur three times within 15 minutes, the CPU will automatically pin 27 changes from Low to High, forward biasing Q681.

Page 26 +12V L623 D624 Q627 R691 C626 T601 (POWER) IC801 C629 RL601 D683 R627 R628 AC IN Q681 R683 C683 D680 POWER L901 ON/OFF PS601 D629 DEGAUSSING POSISTOR (20V) COIL R629 TIME IC681 BASE ALWAYS TIME BASE +5V REG C258 C497 R498 +7.6V D801...

Page 27: Tv/Av Switching Circuits

TV/AV SWITCHING CIRCUITS The VB7C chassis (AVM-2780G) provides for the input of Auxiliary Video and The selection of the AV1 S-Video, AV1 Composite Video, or AV2 Video signal Audio signals. is controlled by the CPU and the mechanical switch of AV1 S-Video input jack K1051.

Page 28 IC101 IC801 IC8001 SIGNAL PROCESSOR PIP SIGNAL PROCESSOR Q8097 BUFFER BUS SDA A101 Q8093 Interface TUNER BUS SCL Interface BUFFER Q8065 BUFFER Q8090 MUTE VIDEO BUFFER DET. TV/AV Q162 Q8076 Q8073 BUFF. BUFFER S1-SW CVBS IN INPUT VIDEO YC SEP MAIN AV1/AV2 FILTER Q1071...

Page 29: Reference Oscillator

REFERENCE OSCILLATOR REFERENCE OSCILLATOR TIME DISPLAY FEATURE The CPU requires a stable oscillator to serve as the clock signal. This clock The C-003 CPU provides a time display feature. The time of day clock is signal will be used to control the timing of all CPU functions and control timed by counting the reference oscillator frequency of 8 MHz served to the pulses.

Page 30: Crt Display Circuit

CRT DISPLAY CIRCUIT The CPU generates and controls all characters and data for the on-screen desired number of clock pulses, the letter signals are output on pins 40-42, displays. Excluding Captions, the VB7C chassis is designed for a green, red, and the blanking signals are output on pin 39.

Page 31: Memory Control Circuit

MEMORY CONTROL CIRCUIT The VB7C chassis is equipped with a nonvolatile memory IC to store certain Control of the memory IC is through CPU pins 31 and 33. information that should remain intact through a power failure. IC802 is the 2K bit serial EEPROM used to store this information.

Page 32 DEVICE CODE WORD DATA n DATA n+1 DATA n+7 ADDRESS(n) CONTROL BYTE READ/WRITE NOTE : ACK=ACKNOWLEDGE BIT Write-In Mode DEVICE CODE WORD DEVICE CODE DATA n DATA n+X ADDRESS(n) CONTROL BYTE CONTROL BYTE READ/WRITE READ/WRITE Read-Out Mode NOTE : ACK=ACKNOWLEDGE BIT –...

Page 33: Momentary Mute Circuit

MOMENTARY MUTE CIRCUIT The Momentary Mute circuit is provided to prevent buzz or static in the When changing channels, the CPU will output the BUS control signals and the speakers when changing channels. The momentary mute circuit operates Mute signal to perform the momentary mute. The BUS control signals from when the power key is pressed, when changing channels, when switching the CPU are input to the BUS Interface circuit within IC3401, the MTS Antenna mode, when searching channels, when changing MTS or TV/AV...

Page 34 IC3401 IC001 IC801 MTS PROCESSOR AUDIO AMP. C002 C010 L881 R881 R3401 SP901 VOL-R VOLUME SPEAKER (R) R3402 L882 CONTROL R882 VOL-L SP902 TREBLE SPEAKER (L) BASS/TREBLE C001 C011 CONTROL BASS MUTE Interface C007 R011 SURROUND to BUS Line SURR BLOCK Q001 FEXT1...

Page 35: Aft Defeat Circuit

AFT DEFEAT CIRCUIT The AFT Defeat circuit is provided to reduce interference or “tweet” in the to turn off the AFT Amplifier, then the AFT output voltage at pin 13 of IC101 video produced by the AFT circuitry. Since the AFT function is needed only will be fixed to 1/2Vcc (approx.

Page 36 FM Trap 7.6V L166 (88.1 ~ 91.9MHz) R164 Internal T131 Video Out X153 FM Coil L164 7.6V Selected External 4.5MHz R133 Video Out Video In X161 R163 R159 VIF VCC C133 R207 C139 Q162 R169 C147 IC101 SIGNAL PROCESSOR R138 TP16 IF In Multiplier...

Page 37: Cpu Reset Operation

CPU RESET OPERATION The CPU must be reset each time AC power is applied. The reset function The reset operation provides two functions for the CPU system First, when ensures that the 5 volt power supply is supplying sufficient power to the CPU, power is first applied to the system the reset circuit will initiate a micro and the crystal-controlled reference oscillator has stabilized before the CPU computer program within the CPU.

Page 38 IC801 ALWAYS L821 C822 C806 R816 D831 R814 (3.6V) Q831 RESET R813 C811 L851 AVCC CPU Reset Circuit AVCC AVCC 4.5 V RESET RESET 2µS 15µS CPU Reset Voltage – 35 –...

Page 39: Automatic Bright Level Adjustment System

AUTOMATIC BRIGHT LEVEL ADJUSTMENT SYSTEM The Automatic Bright Level Adjustment System employed in the VB7C The automatic bright level adjustment system is composed of the beam chassis replaces the mechanically adjusted Sub-Bright Level control used in current detection circuit and the automatic adjustment program in the CPU. conventional systems.

Page 40 Tuner Voltage Signal Converter Memory Processor (L.P.F) Sub-Bright Level Receiver Control Transmitter Conventional Bright Level Adjustment System A101 Special Signal Tuner Input A/D Input Voltage at 0 beam current 57/128 Vcc IC101 Signal Processor 53/128 Vcc Standard Voltage: A IC801 Brightness IC802 Data...

Page 41 AUTOMATIC BRIGHT LEVEL ADJUSTMENT SYSTEM (Continued) When the command data for the Automatic Bright Level Adjustment is input The CPU will begin decreasing the reference voltage from 125/128 Vcc (31/31 from the remote control, the CPU starts the automatic adjustment program. steps) sown to 21/128 Vcc (5/31 steps) by 2steps (8/128 Vcc) until the reference voltage becomes just lower than the A/D input voltage.

Page 42 Enter Automatic Adjustment mode Wait for 100 msec Time Base signal at CPU pin 26 is High ? (Error) Preset BUS Data Outputs to eliminate beam current: BRIGHTNESS 0/127* , CONTRAST 0/64 ... 0/127 = 0/63 for Bright Level Adjustment + 0/64 for Customer Control Wait for 1 sec Read A/D Input Voltage at CPU pin 30 A/D Input Voltage...

Page 43: Automatic Rf Agc Adjustment System

AUTOMATIC RF AGC ADJUSTMENT SYSTEM The Automatic RF AGC Adjustment System employed in the VB7C chassis The automatic RF AGC adjustment system is composed of the RF AGC A/D replaces the mechanically adjusted RF AGC control used in conventional (Analog/Digital) input circuit, the automatic adjustment program in the CPU systems.

Page 44 VIF/SIF Processing Circuit Tuner Video/Chroma Video Video Processing Amp. Detector Amp. Circuit Level Audio Processing Speaker Circuit IF VCC RF AGC Control l Conventional RF AGC Adjustment System Special Signal Input IC101 Signal Processor This curve can be moved to A101 (VIF/SIF Processing Circuit) right or left by the RF AGC...

Page 45 AUTOMATIC RF AGC ADJUSTMENT SYSTEM (Continued) When the command data for the Automatic RF AGC Adjustment is input from When the A/D input voltage is between 69/128 Vcc (2.70V) and 85/128 Vcc the remote control, the CPU starts the automatic adjustment program. (3.32V), the RF AGC adjustment is determined to have been normally completed and the BUS data in the RF AGC Delay Control Register is memorized into IC802, the Memory IC.

Page 46 Enter Automatic Adjustment mode Preset BUS Data for RF AGC Delay Control to "011001" (25/64 steps) Output BUS Data for RF AGC Delay Control Wait for 100 msec A/D Input Voltage 3.32V ? Add 1 step (1/64) from BUS Data for RF AGC Delay Control >...

Page 47: Closed-Captioning Description

CLOSED-CAPTIONING DESCRIPTION The VB7C chassis provides for the decoding and displaying the latest Closed- Text Captioning information transmitted with many of today’s television broadcasts. Text is non-video related information and is displayed in a black box which overwrites the screen. In a full screen Text mode the box is 15 rows high and Captioning is a printed version of the program sound or other information 34 columns wide.

Page 48 Start Bit CLOCK PULSE in BURST Clock Run-in Character 1 Character 2 (7 Cycles) Odd Field Program H-sync Color Burst Line 21 Field 1 Encoded Composite Data Signal – 45 –...

Page 49: The Closed-Caption Decoder Section

THE CLOSED CAPTION DECODER SECTION The closed-caption decoder system used in the VB7C type chassis is capable On Screen Display of processing and displaying all of the latest standard line 21 closed-caption The OSD block interprets the digital data signal input from the Data Slicer transmissions.

Page 50 IC801 CPU(C-003) C853 R854 Composite OSD Control Registers Data Slicer Video signal C854 R853 (address 00D0 OSD Control Register DATA SLICER CLOCK Horiz. Position Register (address 00D1 (27MHz) Block Control Register (address 00D2 00D3 OSC1 Vert. Position

Register (address 00D4 00D5 OSC2 Window Register...

Page 51: Caption Data Slicer

CAPTION DATA SLICER The Data Slicer extracts the caption data encoded on ling 21, field 1 (odd) of SYNC SEPARATOR, TIMING GENERATOR the composite video signal for input into the OSD Controller included in the The composite sync signal from the Sync Slicer is input to the Sync Separator CPU.

Page 52 IC801 CPU(C-003) Horizontal HSYNC Sync Signal C856 R851 C857 C853 R854 CVIN Composite Video Signal R853 C854 VHOLD C858 Caption Data Slicer Block Diagram – 49 –...

Page 53 CAPTION DATA SLICER (Continued) REFERENCE VOLTAGE GENERATOR, COMPARATOR 16-BIT SHIFT REGISTER The Reference Voltage Generator generates the reference voltage The output signal from the Comparator is stored in the 16-Bit Shift Register corresponding to the amplitude of Clock Run-In Burst in line 21 field 1 of the only when the data clock is output.

Page 54 Hsep Clock Run-In Start Bit + 16 Data Video Signal Window The presence of the Clock Run-In is determined by the number (4 - 6) of Clock Run-In pulses in the Window. Caption Data (Enlarged) Video Signal Caption Data Vertical Interval Composite Video Line 21...

Page 55: F/S Tuning System Description

F/S TUNING SYSTEM DESCRIPTION The C-003 Frequency Synthesizer Tuning System is similar to previous PLL In operation, the tuner is precisely adjusted to the frequency of the channel (Phase Locked Loop) systems described in earlier training manuals. The selected by phase comparing (after frequency division) the tuner local primary difference between this system and previous systems is that much of oscillator frequency with a crystal controlled oscillator reference frequency in the system has been integrated into a single IC and included in the Tuner.

Page 56 PLL Data Format Table 1. Address Byte Voltage applied to the Address (MSB) (LSB) COMMAND BYTE DATA BYTE Address Input (ADSW) of Tuner Address byte (ADB) MA1 MA0 C0 h 0 to 0.5V Divider byte 1 (DB1) Divider byte 2 (DB2) Control byte (CB) Table 2.

Page 57: Pll Operation

PLL OPERATION The UHF/VHF tuner local oscillator signal is input to the programmable divider The 4 MHz crystal controlled oscillator outputs is divided by 512 to provide the of the MIX-OSC/PLL IC (CXA3135AN). reference frequency of 7.8125 KHz. This reference frequency from the divider is input to the phase comparator.

Page 58 TUNER CHARGE PUMP OUT LOCK (CXA3135AN) UHF/VHF BUFFER LOCAL OSC LOCAL BAND SW PRESCALER BAND SW CHARGE LOCK DRIVER PUMP DET. PHASE MAIN COUNTER SWALLOW COMPARATOR COUNTER 9-bit 5-bit PROGRAMMABLE 7.8125 KHz 7.8125 KHz DIVIDER 14-bit 4-bit REF. DIVIDER 1/512 4 MHz C BUS 18-bit SHIFT...

Page 59: Pip Control Circuits

PIP CONTROL CIRCUIT The AVM-2780G provides for Picture In Picture (PIP) function through CPU, the horizontal and vertical sync circuits, the PIP sync separation circuit IC8001, the PIP Signal Processor IC. and the PIP 3.3 VDC supply circuit. There are two inputs from CPU; the SDA The PIP circuits perform PIP On/Off, PIP Swap, PIP Location, PIP Freeze and (Serial Data) input/output from pin 32, and the SCL (Serial Clock) input from PIP Select functions.

Page 60 IC801 3.3V R8002 Q8000 L8036 R8036 POWER ON RESET R8001 R8009 C8036 C8002 IC8001 D8000 (3.9V) L8070 SIGNAL PROCESSOR R8092 Q8093 C8072 R8093 R8091 R8089 Q8090 R8090 L8094 R8096 Q8097 R8097 L8036 R8095 3.3V R8088 R8005 L8098 Q8005 MAIN PIX H-SYNC R8003 L8007 R8006...

Page 61: Pip Circuits

PIP CIRCUITS The new YC Picture In Picture (PIP) system employed on the VB7C (AVM- PIP Signal Processor 2780G) is different from the previous PIP system on the VB7A chassis. The The PIP Signal Processor IC8001 is composed of the sub-picture Y/C primary difference between this system and the previous system is that the V- processing circuits and the Y/C Input/Output Switch.

Page 62 TV ANT IC101 IC801 SIGNAL PROCESSOR CSYNC(s) BGP(s) IC8001 /TEST1 /TEST0 Q1071 PIP SIGNAL PROCESSOR BUFFER BUS SDA Y in A101 Y-PIP Interface TUNER BUS SCL Q8065 Sync tip BUFFER Clamp C in VIDEO Bias C-PIP DET. Q162 TV/AV Vdd/Vss S1-SW Q8097 for test...

Page 63: Mts Circuit

MTS CIRCUIT (1) L+R (MAIN) The variable de-emphasis circuit transmittance and VCA gain are After the audio multiplexing signal input from COMPIN (Pin 13) passes respectively controlled by each of effective value detection circuits. Each through MVCA, the SAP signal and telemetry signal are suppressed by of the effective value detection circuits passes the input signal through a STEREO LPF.

Page 64 C BUS DECODER 0û PILOT 90û MODE (VCO 8f PEAK DEV 0û CONTROL AM-DSB-SC STEREO LPF MAIN LPF DE.EM (COMPIN) (MAIN OUT) (MAIN IN) PILOT MVCA CANCEL 4.7µ L + R WIDEBAND SUB LPF (SUBOUT) (ST IN) MATRIX L-R (DSB) SUBVCA (Lch) dbx-TV...

Page 65: Color Enhancer Control Circuit

COLOR ENHANCER CONTROL CIRCUIT Model AVM-2780G provides for a Color Enhancer function. The Color Register and subtracting 8 steps (8/127) or the BUS data for the B-Drive Enhancer function is selected by using the on-screen menu. The Color Control Register. However, if the result in the addition or the subtraction of Enhancer circuits perform color temperature selection.

Page 66: Comb Filter

COMB FILTER The VB7C chassis (AVM-2780G) provides for the 2-line digital Y/C separation (5) Dynamic Comb Filter (DCF) IC to separate luminance (Y) and chrominance (C) signals from the composite This block is logical comb filter to extract the chrominance signal. Filtering video signal by using 2 horizontal (H) lines separation.

Page 67: Switching Power Supply

SWITCHING POWER SUPPLY The switching power supply circuits employed in the VB7C chassis is (I) Off operation comprised of four blocks: the smoothing circuit, oscillating circuit, control • When control circuit is not operating: circuit and rectified output circuit as shown is Figure 1 below. Because the feedback voltage is determined by the turn ratio of input coil to feedback coil, it is constant when the DC input voltage from C609 is stable.

Page 68 IC801 (12V) T601 D694 IC681 D621 C622 D683 POWER ALWAYS L621 R604 R621 R603 R606 R620 D610 C620 D627 C608 L623 Q627 L601 RL601 C626 D624 C481 C629 R627 R691 (12V) Q601 R628 Q681 R683 C683 POWER ON/OFF D680 PS601 D625 C628 L901...

Page 69 collector, the output from the photo diode inside D612 will also increase. The (lll) On Operation (T2 Period in Figure 2) The current produced from the output coils decreases in inverse proportion to output of this photo diode will be received by its photo transistor and the time and when it reaches 0, T1 period finishes and T2 period begins.

Page 70 Q601 OFF PERIOD Q601 OFF PERIOD Q601 ON OPERATION Q601 ON OPERATION Q601 ON PERIOD Q601 ON PERIOD (E) T601 (A) Q601 COLLECTOR TERMINAL EMITTER VOLTAGE CURRENT (F) T601 (B) T601 TERMINAL TERMINAL VOLTAGE OUTPUT CURRENT VOLTAGE RESONANT CURRENT (C) Q601 (G) Q604 BASE ~ EMITTER COLLECTOR...

Page 71 (lll) Other Operation • R614, C612 and D609: During the On operation of Q601, D609 cannot be conductive if the positive • D611 and R616: When the AC input voltage increases, the feedback voltage produced from the feedback voltage is lower than 0.6V. However, during the lower positive feedback coil pins 2 to 3 also increases in direct proportion to the AC input feedback voltage, the current goes through R614 and C612, and turns Q601 voltage.

Page 72 POWER SAVING CIRCUIT As a result, the oscillation of the power supply circuits will stop and the output The power supply circuits employed in the VB7C chassis are equipped with voltages of the power supply circuits will fall down. Also the voltage at point the interval oscillation circuit for saving the power consumed during the stand- (A) will gradually fall down from 12V.

Page 73: Cpu Troubleshooting Hints

CPU TROUBLESHOOTING HINTS Described in this section are some suggested techniques for discovering No Remote Operation (Manual Operation OK) defects in the frequency synthesizer and CPU controlled circuits. An isolation 1. Check for 5 volts on pin 2 of RC Pre-Amp (A1901). transformer should always be used when servicing the TV to prevent possible 2.

Page 74

No MTS Function Color Enhancer 1. While receiving known stereo and SAP signals, check for audio output 1. With an oscilloscope, check for R and B output signals on pins 28 and 30 signals on pins 3, 4, 38 and 39 of IC 3401 with and oscilloscope. of IC101 when selecting “Warm”...

Page 75

(I) H-SYNC (I) V-SYNC (I) POWER FAIL MAIN S SELECT MUTE MAIN AV1/AV2 PIP AV1/AV2 (I) STATUS PIP TV/AV (I) S2 DEFEAT SW MAIN TV/VIDEO (–) KEY SCAN IN (I) BUS SCL (–...

This manual is also suitable for:

Avm-2580gAvm-2759sAvm2760sAvm-2780gAvm-3259gAvm3260g ... Show all