Sanyo LC78626KE Manual

Dsp for compact disk players

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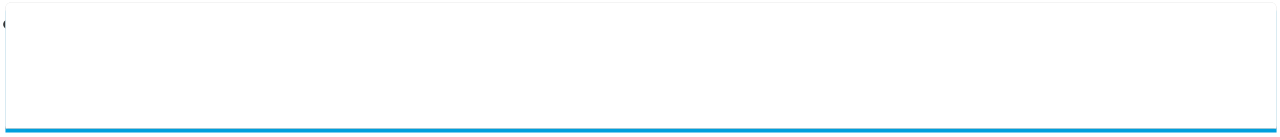

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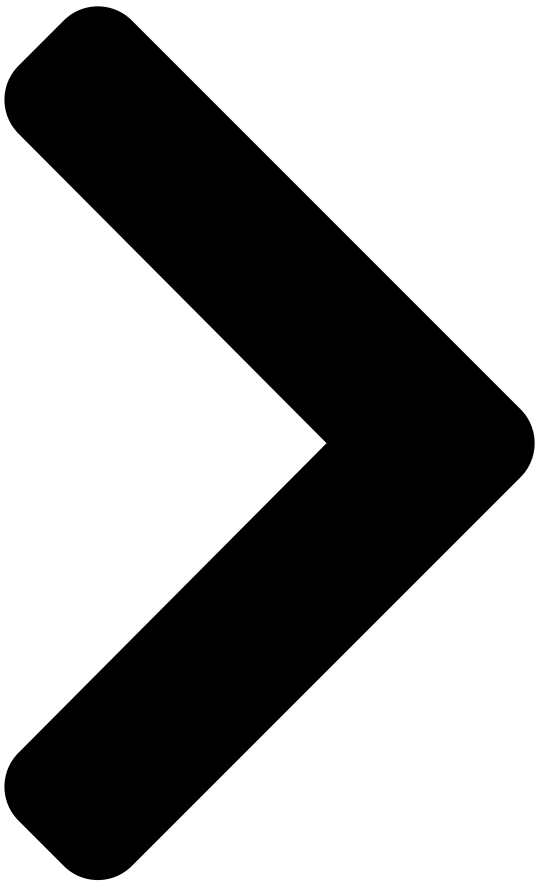


Ordering number : EN5995

Overview

The LC78626KE is a monolithic compact disk player signal processing and servo control CMOS IC equipped with an internal anti-shock control function. Designed for total functionality including support for EFM PLL, and one-bit D/A converter, and containing analog low-pass filter, the LC78626KE provides optimal cost-performance for low-end CD players that provide anti-shock systems by eliminating as many unnecessary features as possible. The basic functions provided by this IC include modulation of the EFM signal from the optical pick-up, deinterleaving, detection and correction of signal errors, prevention of a maximum of approximately 38 seconds of

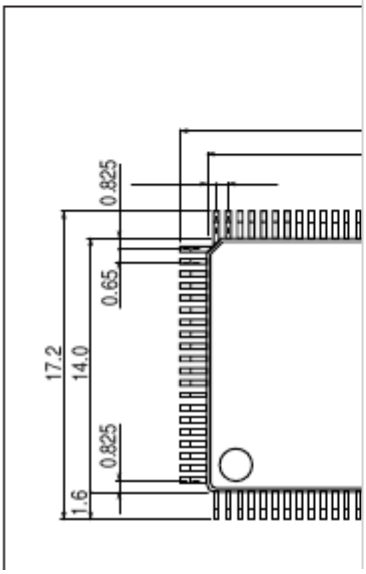
skipping, signal processing such as digital filtering (which is useful in reducing the cost of the player), and processing of a variety of servo-related commands from the microprocessor. The LC78626KE is an improved version of the LC78626E. It provides 8× oversampling digital filters and supports up to 16M of DRAM.

Functions

• When an HF signal is input, it is sliced to precise levels and converted to an EFM signal. The phase is compared with the internal VCO and a PLL clock is reproduced at an average frequency of 4.3218 MHz.
• Precise timing for a variety of required internal timing needs (including the generation of the reference clock) is produced by the attachment of an external 16.9344 MHz crystal oscillator.
• The speed of revolution of the disk motor is controlled by the frame phase difference signal generated by the playback clock and the reference clock.
• The frame synchronizing signal is detected, stored, and interpolated to insure stable data read back.

DSP for Compact Disk Players

• The EFM signal is demodulated and converted to 8-bit symbolic data.
• The demodulated EFM signal is divided into subcodes and output to the external microprocessor. (Three general I/O ports are shared [exclusively] for this purpose.)
• After the subcode Q signal passes the CRC check, it is output to the microprocessor through a serial transmission (LSB first).
• The demodulated EFM signal is buffered in the internal RAM, which is able to absorb ±4 frame's worth of jitter resulting from variations in the disk rotation speed.
• The demodulated EFM signal is unscrambled to a specific sequence, and deinterleaving is performed.



Package Dimensions

unit: mm

3151-QFP100E

[LC78626KE]

0.65
0.575
80
81
100
1

CMOS IC

LC78626KE

Continued on next page.

23.2
20.0
1.6
0.575
0.3
0.15
51
50
31
30
2.7
21.6
0.8

SANYO: QFP100E (QIP100E)

0.1

Table of Contents

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Related Manuals for Sanyo LC78626KE

Turntable Sanyo TP220 Service Manual

(8 pages)

Turntable Sanyo TP 1400 Service Manual

(7 pages)

Turntable Sanyo TP1010UM Service Manual

(8 pages)

Turntable Sanyo TP X2 Operating Instructions Manual

Full automatic belt drive turntable with strobe (7 pages)

Turntable Sanyo TP 1024 Service Manual

Stereo (9 pages)

Turntable Sanyo TP 250 Service Manual

(8 pages)

Turntable Sanyo TP M15 Service Manual

Dc-servo belt drive electronic control full-automatic turntable (16 pages)

Turntable Sanyo TP20 Service Manual

(9 pages)

Turntable Sanyo TPX3 Service Manual

(9 pages)

Turntable Sanyo TP 1012 Instruction Manual

Direct drive stereo turntable (12 pages)

Turntable Sanyo TP 477 Service Manual

(8 pages)

Turntable Sanyo DC X900 Instruction Manual

Cd stereo sound system belt drive turntable (20 pages)

Turntable Sanyo expert TP-1012 Service Manual

(9 pages)

Turntable Sanyo TP1005 Service Manual

Stereo (9 pages)

Turntable Sanyo TP DJ1 Service Manual

Semi-automatic turntable (4 pages)

Summary of Contents for Sanyo LC78626KE

Page 1 SANYO: QFP100E (QIP100E) Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage.

Page 2: Pin Assignment

LC78626KE Continued from preceding page. • A ΔΣ-type D/A converter using a 3-order noise shaper is • Error detection and correction is performed, as is a flag process. (C1: two error/C2: two error correction equipped internally. (An analog low-pass filter is method.)

Page 3 LC78626KE Equivalent Circuit Block Diagram No. 5995-3/34...

Page 4: Specifications

LC78626KE Specifications Absolute Maximum Ratings at Ta = 25°C, V = 0V Parameter Symbol Conditions Ratings Unit Maximum power supply voltage – 0.3 to V + 4.0 Input voltage – 0.3 to V + 0.3 Output voltage – 0.3 to V + 0.3...

Page 5 A filter LCHO, RCHO; 1 kHz: Uses the 0 dB data Cross talk input and the 20 kHz-LPF (in the AD725D) Note: Measured with the normal-speed playback mode in the Sanyo one-bit D/A converter block reference digital attenuator circuit. No. 5995-5/34...

Page 6 LC78626KE Figure 1 Command Input Figure 2 Subcode Q Output Figure 3 Subcode Output No. 5995-6/34...

Page 7 LC78626KE Figure 4 General Port Input Timing Figure 5 General Port Output Timing No. 5995-7/34...

Page 8: Description Of Pins

LC78626KE Description of Pins Output pin states Function Name during reset DEFI Defect detection signal (DEF) input. When not used, must be connected to 0 V. — Test input. Equipped with internal pull-down resistor. Must be connected to 0V. —...

Page 9 LC78626KE Continued from preceding page. Output pin states Description Name during reset General I/O pin 3. This controls the commands from the microcontroller. This pin is shared exclusively with the subcode read clock input (SBCK). When not used, either set this as an input port and connect to 0 V, or...

Page 10 LC78626KE Continued from preceding page. Output pin states Description Name during reset MMC0 Remaining DRAM output Low-level output MMC1 Remaining DRAM output Low-level output MMC2 Remaining DRAM output Low-level output MMC3 Remaining DRAM output Low-level output DRAM write terminated. (An RZP pulse is output when there is an overflow or a shock.)

Page 11 LC78626KE Pin Applications The HF Signal Input Circuit Pin 18: EFMI, Pin 17: EFMO, Pin 1: DEFI, and Pin 20: CLV When an HF signal is input to the EFMI, an EFM signal (NRZ), sliced at the optimal levels, is obtained.

Page 12 LC78626KE The Servo Command Functions Pin 62: RWC, Pin 63: COIN, Pin 64: CQCK Various commands can be executed by setting RWC to high and by inputting the command from COIN synchronized with the CQCK clock. The commands are executed beginning with the falling edge of RWC.

Page 13 LC78626KE The CLV Servo Circuit Pin 20: CLV+, Pin 21: CLV-, Pin 22: V/P Code COMMAND RES = low DISC MOTOR START (Accelerate) DISC MOTOR CLV (CLV) DISC MOTOR BRAKE (Decelerate) DISC MOTOR STOP (Stop) – is the signal for accelerating the disk in the forward direction, while CLV is the signal for decelerating the disk.

Page 14 LC78626KE • Switching the phase control gain Code COMMAND RES = low CLV phase comparator 1/2 frequency division CLV phase comparator 1/4 frequency division CLV phase comparator 1/8 frequency division CLV phase comparator, no frequency division By changing the frequency division value of the first-stage frequency divider of the phase comparator it is possible to change the phase control gain.

Page 15 LC78626KE • Internal brake mode Code COMMAND RES = low Internal Break ON Internal Break OFF Internal brake control Internal brake continuous mode Internal brake continuous mode reset Internal brake TON mode Internal brake TON mode reset * The internal brake mode is turned on by inputting the internal brake on command ($C5). When in this mode, when the brake command ($06) is executed it becomes possible to monitor the state of deceleration of the disk using the WRQ pin.

Page 16 LC78626KE • The TJ command Code COMMAND RES = low The conventional track jump The new track jump 1 TRACK JUMP IN #1 1 TRACK JUMP IN #2 1 TRACk JUMP IN #3 1 TRACK JUMP IN #4 2 TRACK JUMP IN...

Page 17 LC78626KE • TJ mode The relationships between the acceleration pulse,

deceleration pulse, and brake interval are as shown in the table below. When in the conventional track jump mode When in the new track jump mode Command 1 TRACK JUMP IN (OUT) #1 233 µs...

Page 18 LC78626KE The THLD signal is generated on the LA9230M, 9240M, 9250M Series side, and causes the tracking error signal to be held during the JP pulse period. * The tracking brake The relationship between the TES, HFL, and TOFF signals during the track jump period c is as shown below. The TOFF signal is generated from the HFL signal with the changing edge of the TES signal.

Page 19 LC78626KE * When the desired number of tracks is entered as a binary number, the track check operation begins with the falling edge of the RWC. * During the track check the TOFF pin becomes high and the tracking loop turns off, and thus there is the need to provide a feed to the feed motor.

Page 20 LC78626KE The Subcode Q Output Circuit Pin 66: WRQ, Pin 62: RWC, Pin 65: SQOUT, Pin 64: CQCK, Pin 15 CS Code COMMAND RES = low ADDRESS FREE ADDRESS 1 It is possible to read the subcode Q from the SQOUT pin by inputting a clock into the CQCK pin. Of the 8-bit subcodes, the “Q”...

Page 21 LC78626KE Bilingual Function Code COMMAND RES = low STO CONT Lch CONT Rch CONT * At reset or when a stereo command ($28) has been entered, Lch and Rch are output, respectively, to Lch and Rch. * When the Lch set command ($29) is entered, the Lch data is output to both Lch and Rch.

Page 22 LC78626KE 44.1 kHz (normal speed), 88.2 kHz (double speed) Start Stop ATT DATA The audio output level = 20 log ——————— [dB] 100H Because, for example, the time that it would take to increase the attenuation level from “00H” to “EEH” using the 4 step-...

Page 23 LC78626KE Interpolation Circuit If, when the error correction circuit cannot correct an error, the erroneous audio data is output without any correction, the result would be excessive noise. In order to reduce this noise, the erroneous data is replaced with a linear approximation based on the correct data on either side of the incorrect data.

Page 24 LC78626KE Single-byte data + $DB PORT I/O SET dn = 1: Set CONTn to be an output pin dn = 0: Set CONTn to be an input pin Where n = 2 to 5 The ports that are set to output pins then they can independently output either high or low levels. The lower four bits (bits 2 to 5) of the single byte of data correspond to the respective ports.

Page 25 LC78626KE Reset Circuit Pin 69: RES When the power supply is turned on, first set this pin low and then set it to high. The muting is set to –∞dB and the disk motor is set to stop. CLV servo relationship...

Page 26 LC78626KE * C1 and C2 corrections Data that has been EFM modulated is written to the internal RAM, the jitters are absorbed, and then, the following processes are performed with uniform timing through the crystal oscillator clock. First, there is error checking and correction as the C1 block, the C1 flag is determined and written to the C1 flag register.

Page 27 LC78626KE High Anti-shock mode: ON Anti-shock mode: OFF A Schematic of the timing of the various signals during the anti-shock operations are shown in the figure below. Beginning of L point search L point because of shock L point because the DRAM is full Track jump Track jump L point is found.

Page 28 LC78626KE Table of Commands Commands with blank columns: Commands that can not be used. Commands with asterisk marks: Commands that are latched (i.e. mode set commands). Commands marked with @ signs: Commands that are shared with the ASP (LA9240M, etc.). Commands in parentheses: Commands that are exclusive for the ASP (reference).

Page 29 LC78626KE Commands with blank columns: Commands that can not be used.Commands with asterisk marks: Commands that are latched (i.e. mode set commands). Commands marked with @ signs: Commands that are shared with the ASP (LA9240M, etc.). Commands in parentheses: Commands that are exclusive for the ASP (reference).

Page 30 LC78626KE Sample Application Circuit No. 5995-30/34...

Page 31: Handling Of Unused Pins

LC78626KE Comparison of CD-DSP Functions Model LC78626KE LC78622E LC78621E LC78625E LC78630E LC78624E Function (LC78626E) (LC78622NE) EFM-PLL Internal VCO Internal VCO Internal VCO Internal VCO Internal VCO Internal VCO FR = 1.2kΩ FR = 1.2kΩ FR = 1.2kΩ FR = 1.2kΩ...

Page 32 LC78626KE Continued from preceding page. Interface When the inputs and outputs of devices of different types are connected, incorrect operation may occur due to discrepancies between the input V and output V values. Insert level shifters between devices that have different supply voltages to prevent device destruction in systems that use dual power-supply systems.

Page 33 ASP IC documentation when designing application software. Other Notes If you have any questions, please do not hesitate to contact your Sanyo representative, or your Sanyo semiconductor sales outlet. Since this IC is specifically designed for use in CD players, its specifications differ from those of standard logic and other general-purpose IC products.

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