
TOSHIBA
TLX9910

Toshiba TXZ+ TMPM4MNFYAFG Reference Manual

32-bit risc microcontroller, clock control and operation mode

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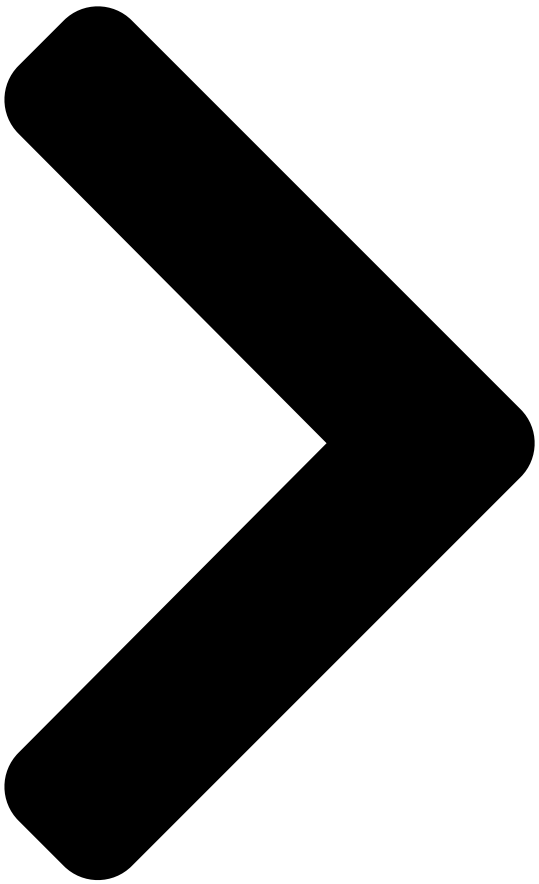

32-bit RISC Microcontroller

TXZ+ Family

TMPM4M Group(1)

Reference Manual

Clock Control and Operation Mode (CG-M4M(1)-E)

Revision 1.1

2022-06

2022-06-24

Toshiba Electronic Devices & Storage Corporation

Rev. 1.1

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Related Manuals for Toshiba TXZ+ TMPM4MNFYAFG

Microcontrollers Toshiba H1 Series Data Book

32bit micro controller tlcs-900/h1 series (751 pages)

Microcontrollers Toshiba TXZ Family Reference Manual

32-bit risc microcontroller txz family reference manual comparator (comp-b) (15 pages)

Microcontrollers Toshiba T6K04 Handbook

Cmos digital integrated circuit silicon monolithic column row driver lsi for a dot matrix graphic lcd (31 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (544 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (652 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Data Book

32bit micro controller (495 pages)

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Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller, serial peripheral inteface tspi-b (67 pages)

Microcontrollers TOSHIBA TXZ Reference Manual

32-bit risc microcontroller (120 pages)

Microcontrollers Toshiba TMP91C824F Data Book

16bit microcontroller tlcs-900/l1 series (255 pages)

Microcontrollers Toshiba TMP96C141AF Manual

Cmos 16-bit microcontroller (178 pages)

Microcontrollers Toshiba TXZ+ TMPM4KLFYAUG Reference Manual

32-bit risc microcontroller (68 pages)

Summary of Contents for Toshiba TXZ+ TMPM4MNFYAFG

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Page 5 TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode List of Figures Figure 1.1 Clock system diagram.....12 Figure 1.2 Mode state transition..... 25 Figure 1.3 NORMAL >>> STOP1 >>> NORMAL Operation mode transition ..... 29 Figure 2.1 TMPM4MxFYA .....44 Figure 2.2 TMPM4MxFWA .....

Page 6: Preface

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Preface Related document Document name ® ® documentation set for the Arm Cortex Exception Oscillation Frequency Detector Voltage Detection Circuit Clock Selective Watchdog Timer Flash Memory The datasheet of each product (Electrical Characteristics) 2022-06-24 6 / 64 Rev.

Page 7: Conventions

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Conventions Numeric formats follow the rules as shown below: Hexadecimal: 0xABC 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers. Decimal: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly Binary: understood from a sentence.

Page 8 TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode

Page 9: Terms And Abbreviations

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Terms and Abbreviations Some of abbreviations used in this document are as follows: Analog to Digital Converter A-ENC32 Advanced Encoder input Circuit (32-bit) A-PMD Advanced Programmable Motor Control Circuit A-VE+ Advanced Vector Engine Plus Controller Area Network Clock Control and Operation Mode Cyclic Redundancy Check...

Page 10: Clock Control And Operation Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1. Clock control and operation mode 1.1. Outlines The clock/mode control block can select a clock gear and prescaler clock, and set the warming-up of oscillator and so on. Furthermore, it has Normal mode and a low power consumption mode in order to reduce power consumption using mode transition.

Page 11: Clock Control

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.2. Clock control 1.2.1. Clock type This section shows a list of clocks: EHCLKIN: The high speed clock input from the external : A clock generated in the internal oscillation circuit or input from the X1 and X2 pins : A clock multiplied with PLL : A clock selected by [CGPLL0SEL]<PLL0SEL>...

Page 12: Clock System Diagram

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.2.3. Clock System diagram The figure below shows a clock system diagram. [CGWUPHCR]<WUON> [CGWUPHCR]<WUPT[15:4]> [CGSPCLKEN] <ADCKEN[3:0]> High speed ADCLK Warming-up

timer [CGWUPHCR] <WUCLK> Peripheral function using fc DNF, OFD(Target clock) [CGOSCCR]<IHOSC1EN> [CGFCEN] <FCIPEN[31:0]>...

Page 13: Warming-Up Function

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.2.4. Warming-up function A warming-up function starts the warming-up timer for high speed oscillator automatically to secure the oscillation stable time when the STOP1 mode is released. It is also available as a count-up timer which uses the warming-up timer for high speed oscillator to secure the stability of an external oscillator or an internal oscillator.

Page 14: The Directions For A Warming-Up Timer

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode The directions for a warming-up timer The directions for a warming-up function are explained. (1) Selection of a clock In a high speed oscillation, the clock classification (an internal oscillation/external oscillation) counted with a warming-up timer is selected by [CGWUPHCR]<WUCLK>.

Page 15: The Formula And The Example Of A Setting Of A Pll Multiplication Value

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode The formula and the example of a setting of a PLL multiplication value The details of the items of [CGPLL0SEL]<PLL0SET[23:0]> which set up a PLL multiplication value are shown below. Table 1.1 Details of [CGPLL0SEL]<PLL0SET[23:0]> setup The items of PLL0SET Function Correction...

Page 16: Change Of The Pll Multiplication Value Under Operation

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode The main examples of a setting of [CGPLL0SEL]<PLL0SET[23:0]> are shown below. It multiplies by PLL, and dividing is carried out and the target Clock frequency (f) is generated for input frequency (f A dividing value is chosen from 1/2, 1/4, and 1/8.

Page 17: Pll Operation Start / Stop / Switching Procedure

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode PLL operation start / stop / switching procedure (1) fc setup (PLL stop >>> PLL start) As an fc setup, the example of switching procedure from the PLL stop state to the PLL operation state is as follows.

Page 18: System Clock

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.2.6. System clock An internal high speed oscillation clock or external high speed oscillation clock (connected oscillator or clock input) can be used as a source of system clock. The system clock consists of "High speed system clock (fsysh)(maximum 160MHz)" for high speed operation and "Middle speed system clock (fsysm)(maximum 80MHz)"...

Page 19: The Setting Method Of A System Clock

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Table 1.7 Operating frequency examples of High speed and Middle speed system clocks Middle speed system High speed clock system clock fsysm (MHz) fsysh (MHz) Note: The maximum frequency of Middle speed system clock is 80 MHz. The setting method of a system clock (1) f setup (Internal oscillation >>>...

Page 20: Osc Setup (Internal Oscillation >>> External Clock Input)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode (2) f setup (Internal oscillation >>> External clock input) As a f setup, the example of switching procedure to the external clock input (EHCLKIN) from an internal high speed oscillator 1(IHOSC1) is shown below. <<...

Page 21: Clock Supply Setting Function

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.2.7. Clock supply setting function This MCU has the clock supply on/off function for the peripheral circuits. To reduce the power consumption, this MCU can stop supplying the clock to the peripheral functions that are not used. Except some peripheral functions, clocks are not supplied after reset.

Page 22: Operation Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.3. Operation mode There are NORMAL mode and a Low Power consumption mode (IDLE, STOP1) in this product as an Operation mode, and it can reduce power consumption by performing mode changes according to directions for use. 1.3.1.

Page 23: Transition To And Return From Low Power Consumption Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Transition to and Return from Low Power Consumption mode In order to shift to each Low Power Consumption mode, the IDLE/STOP1 mode is chosen by standby control register [CGSTBYCR]<STBY[1:0]>, and a WFI (Wait For Interrupt) command is executed. When the transition to the low power consumption mode has been done by WFI instruction, the return from the mode can be done by the reset or an interrupt generation.

Page 24: The Peripheral Function State In A Low Power Consumption Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode The peripheral function state in a Low Power Consumption mode The following Table 1.10 shows the Operation State of the peripheral function (block) in each mode. In addition, after reset release, it will be in the state where a clock is not supplied except for some blocks. If needed, set up [CGFSYSENA],[CGFSYSMENA],[CGFSYSMENB],[CGFCEN],[CGSPCLKEN] and enable clock supply.

Page 25: Mode State Transition

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.3.2. Mode state transition Reset After reset,the internal high- After reset, the internal high speed oscillator (IHOSC) speed oscillator 1 (IHOSC1) oscillates. oscillates. (Note 2) Interrupt STOP1 mode NORMAL (CPU stops except mode some peripheral functions)

Page 26: Stop1 Mode Transition Flow

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode STOP1 mode transition flow Set up the following procedure at switching to STOP1. Because STOP1 mode is released by an interrupt, set the interrupt before switching to STOP1 mode. For the interrupts that can be used to release the STOP1 mode, refer to "1.3.3.1.

Page 27: Return From A Low Power Consumption Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.3.3. Return from a Low Power Consumption mode The release source of a Low Power Consumption mode Interrupt, Non-Maskable Interrupt, and reset can perform return from a Low Power Consumption mode. The standby release source which can be used is decided by a Low Power Consumption mode.

Page 28: Warming-Up At The Release Of Low Power Consumption Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode ● Released by an interrupt request When interrupt cancels a Low Power Consumption mode, it is necessary to prepare so that interrupt may be detected by CPU. The interrupt used for release in STOP1 mode needs to set up CPU, and needs to set up detection by INTIF.

Page 29: Clock Operation By Mode Transition

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.3.4. Clock operation by mode transition The clock operation in case of mode transition is shown below. NORMAL >>> IDLE >>> NORMAL Operation mode transition CPU stops at IDLE mode. The clock supply to a peripheral function holds a setting state. Please perform operation/stop by the register of each peripheral function, a clock supply setting function, etc.

Page 30: Explanation Of A Register

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.4. Explanation of a register 1.4.1. Register list The register related to CG and its address information are shown below. Peripheral function Channel/Unit Base address Clock Control and Operation Mode 0x40083000 Register name Address (Base+) CG write protection register...

Page 31: Detail Of Register

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.4.2. Detail of Register [CGPROTECT] (CG write protection register) Bit Symbol After reset Type Function 31:8 Read as "0". Control write-protection for the CG register (all registers except for this register) PROTECT[7:0] 0xC1 0xC1:...

Page 32: Cgsyscr] (System Clock Control Register)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Note4: To wait stabilizing oscillation of an internal high speed oscillator 1 (IHOSC1) , use a warming-up timer and confirm [CGWUPHCR]<WUEF> instead of <IHOSC1F>. [CGSYSCR] (System clock control register) Bit Symbol After reset Type Function...

Page 33: Cgstbycr] (Standby Control Register)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode [CGSTBYCR] (Standby control register) Bit Symbol After reset Type Function 31:2 Read as "0". Selects a low power consumption mode. 00: IDLE STBY[1:0] 01: STOP1 10: Reserved 11: Reserved [CGPLL0SEL] (PLL selection register for fsys) Bit Symbol After reset Type...

Page 34: Cgwuphcr] (High Speed Oscillation Warming-Up Register)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode [CGWUPHCR] (High speed oscillation warming-up register) Bit Symbol After reset Type Function Sets the upper 12 bits of the 16 bits of calculation values of the warming-up timer. 31:20 WUPT[15:4] 0x800 About a setup of a warming-up timer, refer to the "1.2.4.1.

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TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Bit Symbol After reset Type Function Clock enable of UART ch3 (TSEL24) IPMENA24 0: Clock stop 1: Clock supply Clock enable of UART ch2 (TSEL23) IPMENA23 0: Clock stop 1: Clock supply Clock enable of UART ch1 (TSEL22) IPMENA22 0: Clock stop...

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TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Bit Symbol After reset Type Function Clock enable of PORT F IPMENA05 0: Clock stop 1: Clock supply Clock enable of PORT E IPMENA04 0: Clock stop 1: Clock supply Clock enable of PORT D IPMENA03 0: Clock stop 1: Clock supply...

Page 37: Cgfsysmenb] (Supply And Stop Register B For Fsysm)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode [CGFSYSMENB] (Supply and stop register B for fsysm) Bit Symbol After reset Type Function Clock enable of SIWDT ch0 IPMENB31 0: Clock stop 1: Clock supply Clock enable of NBDIF IPMENB30 0: Clock stop 1: Clock supply IPMENB29...

Page 38: Cgfsysena] (Supply And Stop Register A For Fsysh)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Bit Symbol After reset Type Function Clock enable of A-ENC32 ch1 IPMENB07 0: Clock stop 1: Clock supply Clock enable of A-ENC32 ch0 IPMENB06 0: Clock stop 1: Clock supply Clock enable of OPAMP Unit A/B/C IPMENB05 0: Clock stop 1: Clock supply...

Page 39: Cgfcen] (Clock Supply And Stop Register For Fc)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode [CGFCEN] (Clock supply and stop register for fc) Bit Symbol After reset Type Function 31:29 Read as "0" Clock enable of DNF Unit C (INT21) FCIPEN28 0: Clock stop 1: Clock supply Clock enable of DNF Unit B (INT08b to 18) FCIPEN27 0: Clock stop...

Page 40: Information According To Product

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.5. Information according to product The information about [CGFSYSMENA], [CGFSYSMENB], [CGFSYSENA] and [CGFCEN] which is different according to each product is shown below. 1.5.1. [CGFSYSMENA] Table 1.13 [CGFSYSMENA] register corresponding to each product Channel No./ Internal connection Bit Symbol...

Page 41: Cgfsysmenb]

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.5.2. [CGFSYSMENB] Table

1.14 [CGFSYSMENB] register corresponding to each product Channel No./ Internal connection Bit Symbol Unit name/ M4MN M4MM M4ML peripheral circuit Port name □ □ □ IPMENB31 SIWDT □ IPMENB30 NBDIF □...

Page 42: Cgfsysena]

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 1.5.3. [CGFSYSENA] Table 1.15 [CGFSYSENA] register corresponding to each product Channel No./ Internal connection Bit Symbol Unit name/ M4MN M4MM M4ML peripheral circuit Port name □ □ □ IPENA01 RAMP □ □...

Page 43: Memory Map

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 2. Memory map 2.1. Outlines The memory maps for TMPM4M Group(1) are based on the Arm Cortex-M4(with FPU) processor core memory map. The internal ROM, internal RAM and special function registers (SFR) of TMPM4M Group(1) are mapped to the Code, SRAM and peripheral regions of the Cortex-M4(with FPU) respectively.

Page 44: Tmpm4Mxfya

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 2.1.1. TMPM4MxFYA - Code Flash 256KB - RAM 24KB - Data Flash 32KB TMPM4MLFYAFG, TMPM4MLFYAUG, TMPM4MMFYAFG, TMPM4MNFYAFG, - Products TMPM4MNFYADFG 0xFFFFFFFF 0xFFFFFFFF Vender-Specific Vender-Specific 0xE0100000 0xE0100000 CPU Register CPU Register Region Region 0xE0000000 0xE0000000...

Page 45: Tmpm4Mxfwa

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 2.1.2. TMPM4MxFWA - Code Flash 128KB - RAM 24KB - Data Flash 32KB TMPM4MLFWAFG, TMPM4MLFWAUG, TMPM4MMFWAFG, TMPM4MNFWAFG, - Products TMPM4MNFWADFG 0xFFFFFFFF 0xFFFFFFFF Vender-Specific Vender-Specific 0xE0100000 0xE0100000 CPU Register CPU Register Region Region 0xE0000000 0xE0000000...

Page 46: Bus Matrix

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 2.2. Bus Matrix TMPM4M Group(1) contains the CPU Core of the main master and sub masters. The sub masters include DMAC controller (DMAC) and NBDIF. Main masters connect to slave ports (S0 to S3) of Bus Matrix. In the bus matrix, master ports (M0 to M9) connect to peripheral functions via connections described as (○) or (●) in the following figure.

Page 47: Structure

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 2.2.1. Structure Single chip mode Cortex M4(with FPU) S-Bus D-Bus I-Bus Code Flash Data Flash (Note) Boot ROM RAM0 RAMP(ch 0) RAM1 IB(INTIF) IMN(INTIF) Clock Clock Synchronous Synchronous circut circut DMAC NBDIF IA(INTIF) RAM2...

Page 48: Single Boot Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Single boot mode Cortex M4(with FPU) S-Bus D-Bus I-Bus Code Flash Data Flash (Note) Boot ROM RAM0 RAMP(ch 0) RAM1 IB(INTIF) IMN(INTIF) Clock Clock Synchronous Synchronous circuit circuit DMAC NBDIF IA(INTIF) RAM2 TSPI OPAMP...

Page 49: Connection Table

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 2.2.2. Connection table Connection of Memory related (1) TMPM4MxFYA Single chip mode Table 2.1 Single chip mode Sub master Main master Start Core Core Core Slave DMAC NBDIF Address S-Bus D-Bus I-Bus □...

Page 50: Table 2.3 Single Chip Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode (2) TMPM4MxFWA Single chip mode Table 2.3 Single chip mode Sub master Main master Start Core Core Core Slave DMAC NBDIF Address S-Bus D-Bus I-Bus □ Fault Fault Fault 0x00000000 Code Flash □...

Page 51: Connection Of Peripheral Function

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Connection of peripheral function Table 2.5 Connection of peripheral function Sub master Main master Core Core Core Start Address Slave DMAC NBDIF S-Bus D-Bus I-Bus 0x40000000 Fault Fault Fault Fault □ □...

Page 52: Reset And Power Supply Control

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 3. Reset and power supply control 3.1. Outlines Function classification Factor Functional Description Reset which occurs at the time of a power supply turning Power On Reset on or turning off. LVD reset Reset which occurs below the set-up voltage Cold reset...

Page 53: Reset By A Power On Reset Circuit (Without Using A Reset_N Pin)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Reset by a Power On Reset Circuit (without using a RESET_N pin) After a supply voltage exceeds the release voltage of a Power On Reset (POR), internal reset is deasserted after "Internal initialization time"...

Page 54: Reset By A Reset_N Pin

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Reset by a RESET_N pin When turn on a power supply, it can control the timing of reset release by using RESET_N pin. After a supply voltage exceeds the release voltage of a Power On Reset and even after "Internal initialization time" elapsed, if the RESET_N pin is "Low", internal reset continues.

Page 55: Figure 3.3 Reset Operation By A Reset_N Pin (2)

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode In case of RESET_N pin input change from "Low" to "High" before "Internal initialization time" elapses, internal reset signal is released after "Internal initialization time" elapses. Please goes up a supply voltage into an operating voltage range before "Internal initialization time" elapses. The CPU operates after internal reset release.

Page 56: Continuation Of Reset By Lvd

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Continuation of reset by LVD When the power supply voltage has not exceeded the LVD release voltage even after "Internal initialization time" elapsed, LVD generates the reset signal and the reset state continues. After the power supply voltage exceeds the LVD release voltage and "LVD detection release time"...

Page 57: Warm Reset

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 3.2.2. Warm reset Warm reset by RESET_N pin When resetting with the RESET_N pin, set the RESET_N pin to "Low" for 17.2 µs or more while the power supply voltage is within the operating range. When the "Low"...

Page 58: Starting In Single Boot Mode

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 3.2.3. Starting in single boot mode Refer to the reference manual "Flash Memory" for the details of "single boot mode". Starting by the RESET_N pin When "Low" is inputted to a BOOT_N pin, if reset is released (a RESET_N pin "Low" to "High"), "Single Boot Mode"...

Page 59: Starting In Single Boot Mode When Power Supply Is Stable

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode Starting in single boot mode when power supply is stable When the supply voltage is stable within an operating voltage range, input "Low" to RESET_N pin for reset longer than "Internal processing time", while "Low" is inputted to the BOOT_N pin. And release reset (RESET_N pin to "High").

Page 60: Power On Reset Circuit

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 3.2.4. Power On Reset Circuit The Power On Reset Circuit (POR) generates a reset signal when the power is turned on or turned off. Note: The Power On Reset Circuit may not operate correctly due to the fluctuation of the power supply. Equipment should be designed with full consideration of the electrical characteristics.

Page 61: Turning Off And Re-Turning On Power Supply

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 3.2.5. Turning off and re-turning on power supply When a power supply is turned off, a power supply voltage must be down gentler gradient than Max value of "Power gradient (V)"...

Page 62: The Reset Factor And The Reset Range

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode The reset factor and the reset range Reset factors and the range initialized are shown in Table 3.1. Table 3.1 The reset factor and the range initialized Reset factors Cold Warm Reset Reset Registers and Peripheral function...

Page 63: Revision History

TXZ+ Family TMPM4M Group(1) Clock Control and Operation Mode 4. Revision History Table 4.1 Revision History Revision Date Description 2021-06-15 First release - 3.2.5. Turning off and re-turning on power supply 2022-06-24 Modified chapter title. Modified Chapter number. Modified description. 2022-06-24 63 / 64 Rev.

Page 64: Restrictions On Product Use

Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for.

This manual is also suitable for:

Cg-m4m(1)-e