



Asus AAEON ACP-1074 User Manual

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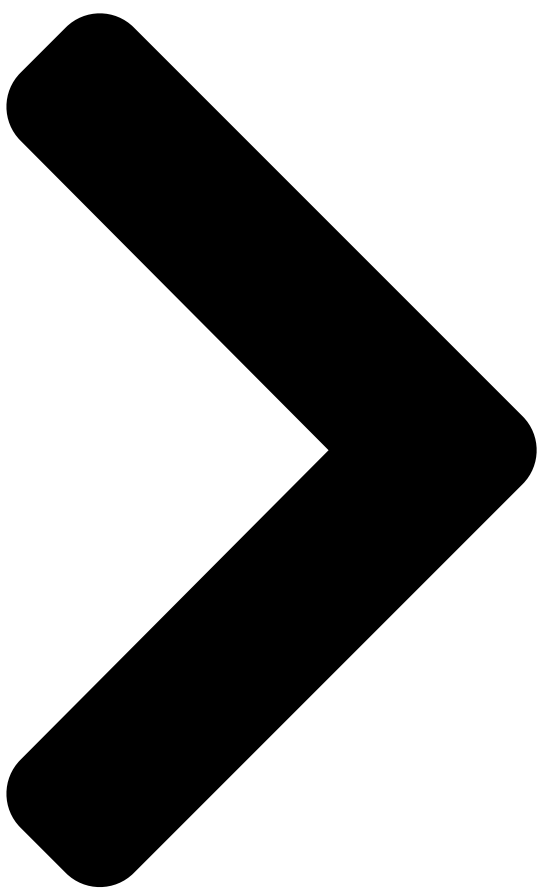
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Infotainment Multi-Touch Panel PC

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User's Manual 2

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Last Updated: February 4, 2016



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Related Manuals for Asus AAEON ACP-1074

[Touch Panel Asus AIO User Manual](#)

(36 pages)

[Touch Panel Asus AAEON ACP-1104 User Manual](#)

Infotainment multi-touch panel pc (91 pages)

[Touch Panel Asus AAEON OMNI-ADP-KIT Series User Manual](#)

Modular touch panel solutions (157 pages)

[Touch Panel Asus AAEON OMNI-2155-CML User Manual](#)

Industrial touch panel with 10th generation intel core processors (103 pages)

[Touch Panel Asus Aaeon BOXER-6403WT User Manual](#)

Fanless embedded box pc (90 pages)

Summary of Contents for Asus AAEON ACP-1074

[Page 1](#) ACP-1074 Infotainment Multi-Touch Panel PC User's Manual 2 Last Updated: February 4, 2016...

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[Page 4](#) Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity ACP-1074 □ RJ-45 COM port cable □ Power adapter □ VESA mount 1 set □ Panel mount 1 set □ Product DVD with User's Manual (in pdf) and drivers □...

[Page 5](#) About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the AAEON.com for the latest version of this document.

[Page 6](#) Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale.

[Page 7](#) As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers. If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii.

[Page 8](#) FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation. Caution: There is a danger of explosion if the battery is incorrectly replaced.

List of Jumpers Please refer to the table below for all of the board's jumpers that you can configure for your application Label Function AT/ATX Mode Selection LVDS BKLT Control Selection LVDS Power Selection LVDS BKLT Control Selection Clear CMOS Jumper Dry and Wet Contact Digital Input Power Selection Dry and Wet Contact Digital Output Power Selection

[Page 24: At/Atx Mode Selection \(Jp1\)](#)

2.2.1 AT/ATX Mode Selection (JP1) 1 2 3 1 2 3 ATX Mode (Default) AT Mode Function ATX Mode (Default) AT Mode 2.2.2 LVDS BKLT Control Selection (JP2) 1 2 3 1 2 3 VR Mode PWM Mode (Default) Function VR Mode PWM Mode (Default) 2.2.3 LVDS Power Selection (JP3)

[Page 25: Lvds Bklt Power Selection \(Jp4\)](#)

2.2.4 LVDS BKLT Power Selection (JP4) 1 2 3 1 2 3 12 V 5 V (Default) Function 12 V 5 V (Default) 2.2.5 Clear CMOS Jumper (JP5) Normal (Default) Clear CMOS Function Normal (Default) Clear CMOS 2.2.6 Dry and Wet Contact Digital Input Power Selection (JP6) 1 2 3 1 2 3 Wet Contact Digital Input...

[Page 26: Dry And Wet Contact Digital Output Power Selection \(Jp7\)](#)

2.2.7 Dry and Wet Contact Digital Output Power Selection (JP7) 1 2 3 1 2 3 Wet Contact Digital Output Dry Contact Digital Output (Default) Function Wet Contact Digital Output Dry Contact Digital Output (Default) Chapter 2 – Hardware Information...

[Page 27: List Of Connectors](#)

List of Connectors Please refer to the table below for all of the board's connectors that you can configure for your application Label Function HDMI Display USB 3.0 Connector COM2 RS-232/422/485 CN16 COM3 RS-232 I/F CN17 COM1 RS-232/422/485 CN22 BIOS SPI Flash Header CN23 Dry and Wet Contact Digital Input CN24...

[Page 28: Hdmi Display \(Cn1\)](#)

2.3.1 HDMI Display (CN1) Pin Name Signal Type Signal Level HDMI_TX2+ DIFF HDMI_TX2- DIFF HDMI_TX1+ DIFF HDMI_TX1- DIFF HDMI_TX0+ DIFF HDMI_TX0- DIFF HDMI_CLK+ DIFF HDMI_CLK- DIFF HDMI_DDC_CLK HDMI_DDC_DATA HDMI_PWR HDMI_HPD Chapter 2 – Hardware Information...

[Page 29: Usb 3.0 Connector \(Cn2\)](#)

2.3.2 USB 3.0 Connector (CN2) Pin Name Signal Type Signal Level USB_D- DIFF USB_D+ DIFF USB3.0 RX- DIFF USB3.0 RX+ DIFF USB3.0 TX- DIFF USB3.0 TX+ DIFF 2.3.3 COM2 RS-232/422/485 Connector (CN4) RS-232 RS-422 RS-485 DATA+ DATA- Chapter 2 – Hardware Information...

[Page 30: Com3 Rs-232 I/F \(Cn16\)](#)

2.3.4 COM3 RS-232 I/F (CN16) RS-232 2.3.5 COM1 RS-232/422/485 Connector (CN17) Chapter 2 – Hardware Information...

[Page 31: Dry And Wet Contact Digital Input \(Cn23\)](#)

RS-232 RS-422 RS-485 DATA+ DATA- 2.3.6 Dry and Wet Contact Digital Input (CN23) Chapter 2 – Hardware Information...

[Page 32](#) Dry Contact Wiring Wet Contact Wiring Digital input voltage range 10 ~ 25 V Pin Name Signal Type Signal Level Digital input 3 Input DRY (5V) WET (3~30V) Chapter 2 – Hardware Information...

[Page 33: Dry And Wet Contact Digital Output \(Cn24\)](#)

Digital input 2 Input DRY (5V) WET (3~30V) Digital input 1 Input DRY (5V) WET (3~30V) Digital input 0 Input DRY (5V) WET (3~30V) WET contact POWER 3~30V 2.3.7 Dry and Wet Contact Digital Output (CN24) Dry Contact Wiring Wet Contact Wiring User I/O Level Digital output voltage range 30 V...

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2.3.8 RJ-45 Ethernet Port (CN26) Pin Name Signal Type Signal Level MDI0+ DIFF MDI0- DIFF MDI1+ DIFF MDI2+ DIFF MDI2- DIFF MDI1- DIFF MDI3+ DIFF MDI3- DIFF 2.3.9 RJ-45 Ethernet Port (CN27) Pin Name Signal Type Signal Level MDI0+ DIFF MDI0- DIFF MDI1+...

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MDI3+ DIFF MDI3- DIFF 2.3.10 USB 2.0 Port 1 Connector (USB1) Pin Name Signal Type Signal Level USB_D- DIFF USB_D+ DIFF 2.3.11 USB 2.0 Port 2 Connector (USB2) Pin Name Signal Type Signal Level USB_D- DIFF USB_D+ DIFF 2.3.12 USB 2.0 Port 3 Connector (USB3) Pin Name Signal Type Signal Level...

[Page 36: Lan1 Connector \(Cn37\)](#)

2.3.13 LAN1 Connector (CN37) Signal Signal MDI0+ MDI0- MDI1+ MDI2+ MDI2- MDI1- MDI3+ MDI3- 2.3.14 DDR3L SODIMM Slot (DIMM1) Standard Specifications 2.3.15 Half Size MiniCard Slot (PCIE1) Pin Name Signal Type Signal Level +3.3V +3.3V +1.5V +1.5V Chapter 2 - Hardware Information...

[Page 37](#) mSATA RX+ DIFF +3.3V +3.3V mSATA RX- DIFF +1.5V +1.5V SMB_CLK +3.3V mSATA_TX DIFF SMB_DATA +3.3V mSATA_TX+ DIFF Chapter 2 - Hardware Information...

[Page 38: Pci-E Full Size Minicard Slot \(Pcie2\)](#)

+3.3V +3.3V +3.3V +3.3V +1.5V +1.5V +3.3V +3.3V 2.3.16 PCI-E Full Size MiniCard Slot (PCIE2) Pin Name Signal Type Signal Level +3.3V +3.3V +1.5V +1.5V Chapter 2 - Hardware Information...

[Page 39](#) PCIE RX- DIFF +3.3V +3.3V PCIE RX+ DIFF +1.5V +1.5V SMB_CLK +3.3V PCIE TX DIFF SMB_DATA PCIE TX+ DIFF Chapter 2 - Hardware Information...

[Page 40: Com-To-Rj-45 Converter Cable \(For Com1 & Com2\)](#)

+3.3V +3.3V +3.3V +3.3V +1.5V +1.5V +3.3V +3.3V 2.3.17 COM-to-RJ-45 Converter Cable (For COM1 & COM2) Chapter 2 - Hardware Information...

[Page 41](#) RS-232 RS-422 RS-485 DATA- DATA+ Chapter 2 - Hardware Information...

[Page 42: Mounting The Panel](#)

Mounting the Panel Step 1: Get the wallmount brackets and sponge ready. Sponge Wall mount bracket Step 2: Remove the six screws (three on each side) at the back and place the wallmount brackets onto the panel. Secure the brackets with the original six screws. Step 3: Place the sponge onto the brackets Sponge Wall mount bracket...

[Page 43](#) wall Step 5: Attach the mounting clips to the four fillisters on the wallmount brackets and tighten the four M4x60 screws to secure the brackets M4x60 screw Mounting clip Chapter 2 - Hardware Information...

[Page 44: Chapter 3 - Ami Bios Setup](#)

Chapter 3 Chapter 3 - AMI BIOS Setup...

[Page 45: System Test And Initialization](#)

System Test and Initialization The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors. The system configuration verification routines check the current system configuration against the values stored in the CMOS memory.

[Page 46: Ami Bios Setup](#)

AMI BIOS Setup The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off. To enter BIOS Setup, press ...

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Setup Submenu: Main Chapter 3 - AMI BIOS Setup...

[Page 48: Setup Submenu: Advanced](#)

Setup Submenu: Advanced Chapter 3 – AMI BIOS Setup...

[Page 49: Advanced: Cpu Configuration](#)

3.4.1 Advanced: CPU Configuration Options summary: Intel Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default EIST Disabled Enabled Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 50: Advanced: Ide Configuration](#)

3.4.2 Advanced: IDE Configuration Options summary: SATA Mode IDE Mode AHCI Mode Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 51: Advanced: Usb Configuration](#)

3.4.3 Advanced: USB Configuration Options summary: Legacy USB Support Enabled Optimal Default, Failsafe Default Disabled Auto Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected Chapter 3 – ...

[Page 52: Advanced: Hardware Monitor](#)

3.4.4 Advanced: Hardware Monitor Chapter 3 – AMI BIOS Setup...

[Page 53: Advanced: Dynamic Digital Io Configuration](#)

3.4.5 Advanced: Dynamic Digital IO Configuration Options summary: GPO0 Direction [Output] Output Level Optimal Default, Failsafe Default GPO1 Direction [Output] Output Level Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

[Page 54: Advanced: Power Management](#)

3.4.6 Advanced: Power Management Options summary: Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select power supply mode. AC Power Loss Last State Optimal Default, Failsafe Default Power On Power Off Select power state when power is re-applied after a power failure. RTC wake system Disabled Optimal Default, Failsafe Default...

[Page 55: Advanced: Sio Configuration](#)

3.4.7 Advanced: SIO Configuration Chapter 3 – AMI BIOS Setup...

[Page 56](#) 3.4.7.1 SIO Configuration: Serial Port 1 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=3F8; IRQ=4; IO=2F8; IRQ=3; Select an optimal setting for IO device Mode: RS232 Optimal Default, Failsafe Default...

[Page 57](#) 3.4.7.2 SIO Configuration: Serial Port 2 Configuration Options summary: Use This Device Disabled Enabled Optimal Default, Failsafe Default En/Disable Serial Port (COM) Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2F8; IRQ=3; IO=3F8; IRQ=4; Select an optimal setting for IO device Mode: RS232 Optimal Default, Failsafe Default...

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Setup submenu: Chipset Chapter 3 – AMI BIOS Setup...

[Page 59: Chipset: North Bridge](#)

3.5.1 Chipset: North Bridge Chapter 3 – AMI BIOS Setup...

[Page 60](#) 3.5.1.1 Display Control Configuration Options summary: Options summary: DVMT Pre-Allocated Optimal Default, Failsafe Default 128M 160M 192M 224M 256M 288M 320M 352M 384M 416M 448M 480M Chapter 3 – AMI BIOS Setup...

[Page 61](#) 512M DVMT Total Gfx Mem 128MB 256MB Optimal Default, Failsafe Default LVDS Panel Type 1024x600, 60Hz Optimal Default, Failsafe Default Color Depth 18 bit Optimal Default, Failsafe Default LVDS Backlight Level 100% Optimal Default, Failsafe Default Chapter 3

- AMI BIOS Setup...

[Page 62: South Bridge](#)

3.5.2 South Bridge Options summary: Audio Controller Disabled Enabled Optimal Default, Failsafe Default Chapter 3 - AMI BIOS Setup...

[Page 63: Security](#)

Security Change User/Administrator Password You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility. Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers).

[Page 64: Setup Submenu: Boot](#)

Setup submenu: Boot Options summary: Quiet Boot Disabled Enabled Default En/Disable showing boot logo. Option ROM Messages Force BIOS Default Keep Current Set display mode for Option ROM Launch PXE OpROM Disabled Default Enabled En/Disable Legacy Boot Option Chapter 3 - AMI BIOS Setup...

[Page 65: Bbs Priorities](#)

3.7.1 BBS Priorities Chapter 3 - AMI BIOS Setup...

[Page 66: Setup Submenu: Exit](#)

Setup submenu: Exit Chapter 3 - AMI BIOS Setup...

[Page 67: Chapter 4 - Drivers Installation](#)

Chapter 4 Chapter 4 - Drivers Installation...

[Page 68: Product Cd/Dvd](#)

Product CD/DVD The ACP-1074 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers. In case the program does not start, follow the sequence below to install the drivers. Step 1 -...

[Page 69](#) Step 4 - Install xHCI Driver (Windows 7 only) Open the Step 4 - xHCI folder and followed by the Setup.exe file Follow the instructions Drivers will be installed automatically Step 5 - Install Intel Sideband Fabric Device Drivers (Windows 8.1/10 only) Open the Step 5 - Intel Sideband Fabric Device followed by the Setup.exe file Follow the instructions...

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Appendix A Appendix A - Watchdog Timer Programming...

[Page 71: Watchdog Timer Initial Program](#)

A.1 Watchdog Timer Initial Program Table 1 : SuperIO relative register table Default Value Note SIO MB PnP Mode Index Register Index 0x2E(Note1) 0x2E or 0x4E SIO MB PnP Mode Data Register Data 0x2F(Note2) 0x2F or 0x4F Table 2 : Watchdog relative register table Register BitNum Value...

[Page 72](#) *****
// SuperIO relative definition (Please reference to Table 1) #define byte SIOIndex //This parameter is represented from Note1 #define byte SIOData //This parameter is represented from Note2 #define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte IOPort); // Watch Dog relative definition (Please reference to Table 2) #define byte TimerLDN //This parameter is represented from Note3 #define byte TimerReg //This parameter is represented from Note4 #define byte TimerVal // This parameter is represented from Note24...

[Page 73](#) *****
VOID Main(){ // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) // (boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure : AaeonWDTEnable // This procedure will enable the WDT counting. AaeonWDTEnable();

[Page 74](#) *****
// Procedure : AaeonWDTEnable VOID AaeonWDTEnable () { WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1); // Procedure : AaeonWDTConfig VOID AaeonWDTConfig () { // Disable WDT counting WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0); // Clear Watchdog Timeout Status WDTClearTimeoutStatus(); // WDT relative parameter setting WDTParameterSetting(); VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value) { SIOBitSet(LDN, Register, BitNum, Value);...

[Page 75](#) *****
VOID SIOEnterMBPnPMode() { IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); VOID SIOExitMBPnPMode() { IOWriteByte(SIOIndex, 0xAA); VOID SIOSelectLDN(byte LDN) { IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN); VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value) { Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData);...

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Appendix C Appendix C - Digital I/O Ports...

[Page 89: Di/O Programming](#)

DI/O Programming ACP-1074 utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application.

[Page 90: Digital I/O Register](#)

Digital I/O Register Table 1 : SuperIO relative register table Default Value Note SIO MB PnP Mode Index Register Index 0x2E(Note1) 0x2E or 0x4E SIO MB PnP Mode Data Register Data

[Page 91: Digital I/O Sample Program](#)

Digital I/O Sample Program

```
***** // SuperIO
relative definition (Please reference to Table 1) #define byte SIOIndex //This parameter is
represented from Note1 #define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte IOPort); //
Digital Input Status relative definition (Please reference to Table 2) #define byte DInput1LDN //
This parameter is represented from Note3 #define byte DInput1Reg // This parameter is
represented from Note4...
```

[Page 92](#) *****

```
// Digital Output control relative definition (Please reference to Table 3) #define byte
DOutput1LDN // This parameter is represented from Note21 #define byte DOutput1Reg // This
parameter is represented from Note22 #define byte DOutput1Bit // This parameter is
represented from Note23 #define byte DOutput1Val // This parameter is represented from
Note24 #define byte DOutput2LDN // This parameter is represented from Note25 #define byte
DOutput2Reg // This parameter is represented from Note26...
```

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```
VOID Main(){ Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read
Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin
level is High PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit); //
Procedure : AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...
```

[Page 94](#) *****

```
Boolean AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){ Boolean PinStatus ;
PinStatus = SIOBitRead(LDN, Register, BitNum); Return PinStatus ; VOID
AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
ConfigToOutputMode(LDN, Register, BitNum); SIOBitSet(LDN, Register, BitNum, Value);
***** Appendix C
- Digital I/O Ports...
```

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```
VOID SIOEnterMBPnPMode(){ IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); VOID
SIOExitMBPnPMode(){ IOWriteByte(SIOIndex, 0xAA); VOID SIOSelectLDN(byte LDN){
IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN);
VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){ Byte TmpValue;
SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue =
IOReadByte(SIOData);...
```

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```
Boolean SIOBitRead(byte LDN, byte Register, byte BitNum){ Byte TmpValue;
SIOEnterMBPnPMode(); SIOSelectLDN(LDN); IOWriteByte(SIOIndex, Register); TmpValue =
IOReadByte(SIOData); TmpValue &= (1 << BitNum); SIOExitMBPnPMode(); If(TmpValue == 0)
Return 0; Return 1; VOID ConfigToOutputMode(byte LDN, byte Register, byte BitNum){ Byte
TmpValue, OutputEnableReg; OutputEnableReg = Register-1;...
```