Asus AAEON BOXER-6840-CFL User Manual

Fanless embedded box pc

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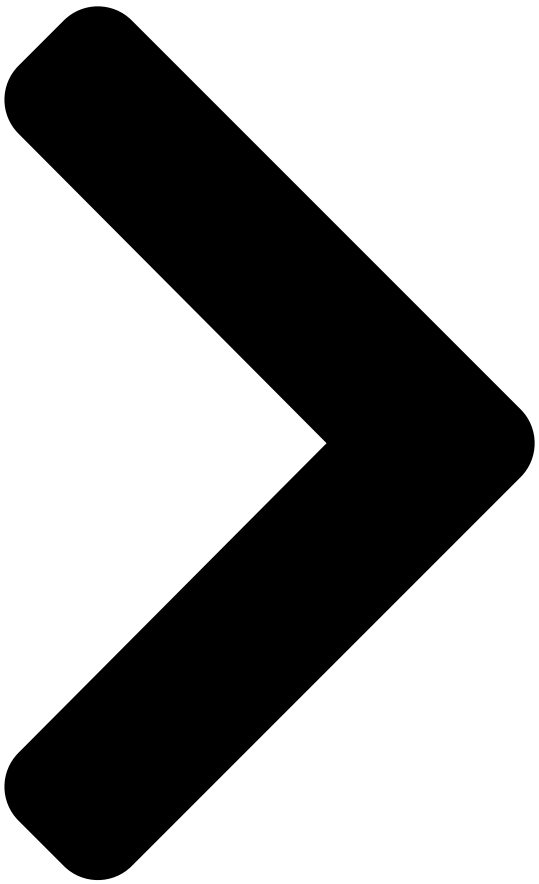

BOXER-6840-CFL

Fanless Embedded Box PC

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User 's Manual 1

Ed

Last Updated: October 7, 2021

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Related Manuals for Asus AAEON BOXER-6840-CFL

Industrial PC Asus AAEON BOXER-6615 User Manual

Fanless embedded box pc (101 pages)

Industrial PC Asus Aaeon BOXER-8331AI User Manual

Embedded ai vision system (108 pages)

Industrial PC Asus AAEON BOXER-6642-CML User Manual

Fanless embedded box pc (112 pages)

Industrial PC Asus Aaeon BOXER-8254AI User Manual

Compact fanless embedded aiaedge box pc with nvidia jetson xavier nx (42 pages)

Industrial PC Asus Aaeon BOXER-6641-A1-1110 User Manual

Fanless embedded box pc (134 pages)

Industrial PC Asus AAEON BOXER-8221AI-B Installation & User Manual

Nvidia jetson nano platform (6 pages)

Industrial PC Asus AAEON BOXER-8623AI User Manual

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Industrial PC Asus AAEON BOXER-8653AI User Manual

Aiaedge compact fanless embedded ai system with nvidia jetson orin nx (49 pages)

Industrial PC Asus AAEON BOXER-6406U-ADN User Manual

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Fanless embedded box pc (104 pages)

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Pico-itx single board computer (105 pages)

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Industrial computer barebone (59 pages)

Industrial PC Asus Aaeon GENESYS-APL7 User Manual

Compact embedded system (85 pages)

Industrial PC Asus AAEON PICO-APL4-SEMI Quick Installation Manual

(3 pages)

Industrial PC Asus EBE-4U User Manual

Industrial computer barebone (69 pages)

Summary of Contents for Asus AAEON BOXER-6840-CFL

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Page 3 Acknowledgement All other product name or trademarks are properties of their respective owners. Microsoft Windows® is a registered trademark of Microsoft Corp. • Intel®, Pentium®, Celeron®, and Xeon® are registered trademarks of Intel • Corporation Intel Core™ is a trademark of Intel Corporation •...

Page 4 Packing List Before setting up your product, please make sure the following items have been shipped: I t em Quantity BOXER-6840-CFL • Wallmount bracket • Screw Package • 3 Pin DC-In Power Connector • If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

Page 5 About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the product page at AAEON.com for the latest version of this document.

Page 6 Saf e ty Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

Page 7 If any of the following situatio ns arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

Page 8 FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation. C aution: There is a danger of explosion if the battery is incorrectly replaced.

Page 9 Chi na RoHS Requirements (CN) □□□□□□□□□□□□□□□□□□ AAEON System QO4-381 Rev.A0 □□□□□□□□□ □□□□ □ □ □ □□□ □□□□ □□□□ □(PBDE) (Pb) (Hg) (Cd) (Cr(VI)) (PBB) □□□□□ × ○ ○ ○ ○ ○ □ □□□□□ □□□□ × ○ ○ ○ ○ ○ □□□□□□...

Page 10 Chi na RoHS Requirement (EN) Hazardous and Toxic Materials List AAEON System QO4-381 Rev.A0 Hazardous or Toxic Materials or Elements Component Name PCB and Components Wires & Connectors for Ext.Connections Chassis CPU & RAM HDD Drive LCD Module Optical Drive Touch Control Module Battery...

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Chapter 1 Chapter 1 - Product Specifications...

Page 16: Specifications

1 .1 Spe cifications System Intel® Xeon® E-2124G CP U Intel® i9-9900T Intel® i7-8700T Intel®

i5-8500T Intel® i3-8100T Pentium® G5400T Celeron® G4900T N o te: Supports max. TDP 71W C246 (no H310 downward support) Chip set DDR4 SO-DIMM socket x 4 (double deck) Sys tem Memory Supports max 2666MHz up to 128GB Supports un-buffered and ECC/non-ECC type...

Page 17 System 1 x Full-Size Mini Card (PCIe + USB with 1 SIM Exp ansion Slot) 1 x Half-Size Mini Card (PCIe + USB, mSATA optional) 1 x M.2 2280 M-Key (PCIe [x4]) 1 x PCIe [x4] 1 x PCIe [x16] N o te: System supports GPU cards up to max 250W TDP N o te: System supports GPU cards max size...

Page 18 E nvironmental -4°F ~ 140°F (-20°C ~ 60°C) IEC68-2 with 0.5 Op erating Temperature m/s airflow St orage Temperature -49°F ~ 176°F (-45°C ~ 80°C) St orage Humidity 5~95% at 40°C, non-condensing A nt i-Vibration with SSD: Random, 1Grms, 5~500Hz Sho ck With SSD: 50G at wall-mount, half-sine, 11ms Certification...

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2.4 Li st of Connectors Please refer to the table below for all of the system’s connectors that you can co nfigure for your application Lab el F unction CN 1 SO-DIMM Channel A0 CN 2 SO-DIMM Channel A1 CN 3 SO-DIMM Channel B0 CN 4 SO-DIMM Channel B1...

Page 28 Lab el F unction CN 24 SATA connector CN 25 SATA PWR connector CN 26 SATA connector CN 27 SATA PWR connector CN 28 DIO box connector CN 29 COM1+COM2 Connector RS232/RS422/RS485 CN 30 COM1 HEADER RS232/RS422/RS485 CN 31 COM2 HEADER RS232/RS422/RS485 CN 32 COM3+COM4 Connector RS232/RS422/RS485 CN 33...

Page 29: Pcie [X4] Slot (Cn5)

Lab el F unction B AT1 RTC Battery Connector 2.4.1 PCIe [x4] Slot (CN5) P in P in Name Sig nal Type Sig nal Level PRSNT1# +12V +V12S +12V +V12S PCIE_TXN5 DIFF PCIE_TXP5 DIFF PCIE_RXN5 DIFF PCIE_RXP5 DIFF +3.3V +V3.3S A 10 +3.3V...

Page 30 P in P in Name Sig nal Type Sig nal Level A 17 PCIE_RXN24 DIFF A 18 A 19 A 20 A 21 PCIE_RXP23 DIFF A 22 PCIE_RXN23 DIFF A 23 A 24 A 25 PCIE_RXP22 DIFF A 26 PCIE_RXP22 DIFF A 27 A 28...

Page 31 P in P in Name Sig nal Type Sig nal Level B 12 B 13 B 14 PCIE_TXP24 DIFF B 15 PCIE_TXN24 DIFF B 16 B 17 PRSNT B 18 B 19 PCIE_TXP23 DIFF B 20 PCIE_TXN23 DIFF B 21 B 22 B 23 PCIE_TXP22...

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Page 34 Dual USB3.0 (USB3.2 Gen 2) P in P in Name Sig nal Type Sig nal Level +5VSB DIFF USB1_D- DIFF USB1_D+ USB1_SSRX− DIFF USB1_SSRX+ DIFF USB1_SSTX− DIFF USB1_SSTX+ DIFF +5VSB DIFF USB2_D- DIFF USB2_D+ USB2_SSRX− DIFF USB2_SSRX+ DIFF USB2_SSTX− DIFF USB2_SSTX+ DIFF Chapter 2 –...

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Page 36 Dual USB3.0 (USB3.2 Gen 2) P in P in Name Sig nal Type Sig nal Level +5VSB DIFF USB3_D- DIFF USB3_D+ USB3_SSRX− DIFF USB3_SSRX+ DIFF USB3_SSTX− DIFF USB3_SSTX+ DIFF +5VSB DIFF USB4_D- DIFF USB4_D+ USB4_SSRX− DIFF USB4_SSRX+ DIFF USB4_SSTX− DIFF USB4_SSTX+ DIFF Chapter 2 –...

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Page 42 P in P in Name Sig nal Type Sig nal Level +3.3V +3.3V DEVSLP RESET# CLKREQ# WAKE# +3.3V +3.3V +3.3V +3.3V +3.3V +3.3V Chapter 2 – Hardware Information...

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RS422_RX- COM Port Select Map: P in Mapping R S-232 R S-485 R S-422 RS422_RX+ (A)

Page 55: Mini Card Slot (Full-Sized) (Cn37)

2.4.25 Mi ni Card Slot (Full-Sized) (CN37) P in P in Name Sig nal Type Sig nal Level PCIE_WAKE# +3.3V +3.3V +1.5V +1.5V PCIE_CLK_REQ# UIM_PWR UIM_DATA PCIE_REF_CLK- DIFF UIM_CLK PCIE_REF_CLK+ DIFF UIM_RESET UIM_VPP W_DISABLE# +3.3V Chapter 2 – Hardware Information...

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Page 58: Mini Card Slot (Half-Sized) (Cn39)

2.4.27 Mi ni Card Slot (Half-Sized) (CN39) P in P in Name Sig nal Type Sig nal Level PCIE_WAKE# +3.3V +3.3V +1.5V +1.5V PCIE_CLK_REQ# PCIE_REF_CLK- DIFF PCIE_REF_CLK+ DIFF W_DISABLE# +3.3V Chapter 2 – Hardware Information...

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P in P in Name Sig nal Type Sig nal Level +1.5V +1.5V +3.3VSB +3.3V 2.4.28 USB2.0 Wafer Box (CN40, CN41, CN42, CN43) N o te: USB2.0 Wafer Box (5P Pitch: 1.25mm) P in P in Name Sig nal Type Sig nal Level USBD- DIFF...

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2.4.29 Audi o Jack Connector (CN44) P in P in Name Sig nal Type Sig nal Level MIC_R LOUT_R HP_DET2 HP_DET3 HP_DET1 LOUT_L MIC_L Chapter 2 – Hardware Information...

Page 62: Audio Connector Wafer Box

2.4.30 Audi o Connector Wafer Box P in P in Name Sig nal Type Sig nal Level MIC_L MIC_R LIN_L LIN_R LOUT_L LOUT_R VDD_AUD Chapter 2 – Hardware Information...

Page 63: Dc-In Connector (Cn48)

2.4.31 DC-IN Connector (CN48) P in P in Name Sig nal Type Sig nal Level 2.4.32 G PU DC-IN Connector (CN50, CN51) P in P in Name Sig nal Type Sig nal Level +12V +12V +12V +12V +12V +12V Chapter 2 –...

Page 64: Rtc Battery Connector (Bat1)

P in P in Name Sig nal Type Sig nal Level +12V +12V 2.4.33 RTC Battery Connector (BAT1) P in P in Name Sig nal Type Sig nal Level +3.3VA_RTC 3.3V Chapter 2 – Hardware Information...

Page 65: Cpu Installation

2.5 CPU Installation Step 1: Power down the system, unplug the power cord and ensure the system is off. Step 2: Have 8 Generation Intel Core, Xeon, Celeron or Pentium CPU ready. See Chapter 1 for processor compatibility. Step 3: Remove the top cover by unscrewing the four retentio n screws. You will see the CPU socket as in Figure 1.

Page 66: Expansion Card Installation

2.6 E xpansion Card Installation Step 1: Power down the system, unplug the power cord and ensure the system is off. Step 2: Have the PCI Express card you wish to install ready, with the rear bracket attached. Step 3: Remove the bottom panel from the system. Note: there are ten

(10) retaining screws.

Page 67 Step 6: Secure the card in place with the sliding bracket as follows: A : Turn the securing screws counter-clockwise to Open. B : Push the middle of the securing bracket down towards the expansion card. Note: the bracket should fit securely but not apply pressure onto the card. C: Lock the securing screws by turning them clockwise.

Page 68 Step 7: Reattach the bottom panel with the ten screws removed in Step 3, as shown in figure 3. Step 8: Attach mounting brackets as shown in figure 4. Chapter 2 – Hardware Information...

Page 69: Chapter 3 - Ami Bios Setup

Chapter 3 Chapter 3 - AMI BIOS Setup...

Page 70: System Test And Initialization

System Test and Initialization The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

Page 71: Ami Bios Setup

3.2 AMI BIOS Setup The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off. To enter BIOS Setup, press <Del>...

Page 72: Setup Submenu: Main

3.3 Se tup Submenu: Main Chapter 3 – AMI BIOS Setup...

Page 73: Setup Submenu: Advanced

3.4 Se tup Submenu: Advanced Chapter 3 – AMI BIOS Setup...

Page 74: Trusted Computing

3.4.1 Trusted Computing Op tions Summary Security Device Enable Optimal Default, Failsafe Default Sup port Disable Enable or Disable BIOS support for security device. TCG EFI protocol and INT1A interface will not be available. SHA-1 PCR Bank Enabled Optimal Default, Failsafe Default Disabled Enable or Disable SHA-1 PCR Bank SHA 256 PCR Bank...

Page 75 Op tions Summary P latform Hierarchy Enabled Optimal Default, Failsafe Default Disabled Enable or Disable Platform Hierarchy St orage Hierarchy Enabled Optimal Default, Failsafe Default Disabled Enable or Disable Storage Hierarchy End orsement Hierarchy Enabled Optimal Default, Failsafe Default Disabled Enable or Disable Endorsement Hierarchy TP M2.0 UEFI Spec TCG_2...

Page 76: Cpu Configuration

3.4.2 CPU Configuration Op tions Summary I nt el (VMX) Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. A ctive Processor Cores Optimal Default, Failsafe Default Number of cores to enable in each processor package.

Page 77 Op tions Summary Turbo Mode Disabled Enabled Optimal Default, Failsafe Default Enable/Disable Processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available or enabled). C s t ates Disabled Optimal Default, Failsafe Default Enabled Enable/Disable CPU Power Management. Allows CPU to go C states when it’s not 100% utilized Chapter 3 –...

Page 78: Pch-Fw Configuration

3.4.3 PCH-FW Configuration Op tions Summary ME State Enabled Optimal Default, Failsafe Default Disabled When Disabled ME will be put into ME Temporarily Disabled Mode. A MT BIOS Feature Enabled Optimal Default, Failsafe Default Disabled When disabled AMT BIOS Features

are no longer supported and user is no longer able to access MEBx Setup.

Page 79: Firmware Update Configuration

3.4.3.1 Fi rmware Update Configuration Op tions Summary ME F W Image Re-Flash Enabled Disabled Optimal Default, Failsafe Default Enable/Disable ME FW Image Re-Flash function. Chapter 3 – AMI BIOS Setup...

Page 80: Ptt Configuration

3.4.3.2 PT T Configuration Op tions Summary ME F W Image Re-Flash dTPM Optimal Default, Failsafe Default Selects TPM device: PTT or dTPM. PTT – Enables PTT in SkuMgr dTPM 1.2 – Disables PTT in SkuMgr Warning! PTT/dTPM will be disabled and all saved data will be lost. Chapter 3 –...

Page 81: Sata Configuration

3.4.4 SATA Configuration Op tions Summary SATA Mode AHCI Mode Optimal Default, Failsafe Default Selection Intel RST Premium With Intel Optane System Acceleration Determines how SATA controller(s) operate. A g gressive LPM Enabled Sup port Disabled Optimal Default, Failsafe Default Enable PCH to aggressively enter link power state.

Page 82: Usb Configuration

3.4.5 USB Configuration Op tions Summary X HCI Hand-off Enabled Optimal Default, Failsafe Default Disabled This is a workaround for OSes without XHCI Hand-off support. The XHCI ownership change should be claimed by XHCI driver. U SB Mass Storage Driver Enabled Optimal Default, Failsafe Default Sup port...

Page 83: Hardware Monitor

3.4.6 Hardware Monitor Op tions Summary Smart Fan Enabled Optimal Default, Failsafe Default Disabled Enable or Disable Smart Fan Chapter 3 – AMI BIOS Setup...

Page 84: Smart Fan Mode Configuration

3.4.6.1 Sm ar t Fan Mode Configuration Op tions Summary Fan 1/2 Output Mode Output PWM mode Optimal Default, Failsafe Default (push pull) Linear Fan Application Output PWM mode (open drain) Output PWM mode (push pull) to control 4-wire fans. Linear fan application circuit to control 3-wire fan speed by fan’s power terminal.

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Op tions Summary Temperature 1/2/3/4 1-100 Range 60/50/40/30 Optimal Default, Failsafe Default Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100 Dut y Cycle 1/2/3/4/5 1-100 Range 85/70/60/50/40 Optimal Default, Failsafe Default Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100 Chapter 3 –...

Page 86: Sio Configuration

3.4.7 SIO Configuration Chapter 3 – AMI BIOS Setup...

Page 87: Serial Port 1 Configuration

3.4.7.1 Se ri al Port 1 Configuration Op tions Summary U s e This Device Enabled Optimal Default, Failsafe Default Disabled Enabled or Disabled this Logical Device. Device resource USB Automatic Setting Optimal Default, Failsafe Default s ettings IO=3F8h; IRQ = 4; IO=2F8h;...

Page 88: Serial Port 2 Configuration

3.4.7.2 Se ri al Port 2 Configuration Op tions Summary U s e This Device Enabled Optimal Default, Failsafe Default Disabled Enabled or Disabled this Logical Device. Device resource USB Automatic Setting Optimal Default, Failsafe Default s ettings IO=2F8h; IRQ = 3; IO=3F8h;...

Page 89: Serial Port 3 Configuration

3.4.7.3 Se ri al Port 3 Configuration Op tions Summary U s e This Device Enabled Optimal Default, Failsafe Default Disabled Enabled or Disabled this Logical Device. Device resource USB Automatic Setting Optimal Default, Failsafe Default s ettings IO=3E8h; IRQ = 11; IO=2E8h;...

Page 90: Serial Port 4 Configuration

3.4.7.4 Se ri al Port 4 Configuration Op tions Summary U s e This Device Enabled Optimal Default, Failsafe Default Disabled Enabled or Disabled this Logical Device. Device resource USB Automatic Setting Optimal Default, Failsafe Default s ettings IO=2E8h; IRQ = 11; IO=3E8h;...

Page 91: Network Stack Config Uration

3.4.8 Ne twork Stack Configuration N etwork Stack Disabled: Op tions Summary N etwork Stack Disabled Enabled Optimal Default, Failsafe Default Enable/Disable UEFI Network Stack Chapter 3 – AMI BIOS Setup...

Page 92 N etwork Stack Enabled: Op tions Summary N etwork Stack Disabled Enabled Optimal Default, Failsafe Default Enable/Disable UEFI Network Stack I p v4 PXE Support Disabled Enabled Optimal Default, Failsafe Default Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Page 93: Digital Io Port Config Uration

3.4.9 Di gital IO Port Configuration Op tions Summary DI O Type Output Optimal Default, Failsafe Default Input Set DIO as Input or Output DI O Data High Optimal Default, Failsafe Default Set is output level when DIO pin is output Chapter 3 –...

Page 94: Power Management

3.4.10 Powe r Management Op tions Summary Po wer Mode ATX Type Optimal Default, Failsafe Default AT Type Select power supply mode. A C Power Loss Last State Optimal Default, Failsafe Default Power On Power Off Select power state when power is re-applied after a power failure. R TC wake system Disabled Optimal Default, Failsafe Default...

Page 95 Op tions Summary Wake up hour Select 0-23; For example: enter 3 for 3am and 15 for 3pm Wake up minute 0 – 59 Wake up second 0 - 59 Chapter 3 – AMI BIOS Setup...

Page 96: Setup Submenu: Chipset

3.5 Se tup Submenu: Chipset Chapter 3 – AMI BIOS Setup...

Page 97: System Agent (Sa) Configuration

3.5 .1 System Agent (SA) Configuration Op tions Summary P rimary Display Auto Optimal Default; Failsafe Default IGFX Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx. SA GV Enabled Optimal Default, Failsafe Default Disabled Fixed Low Fixed High...

Page 98 Op tions Summary R C6(Render Standby) Enabled Optimal Default, Failsafe Default Disabled Check to enable render standby support. DVMT Total Gfx Mem 128M 256M Optimal Default, Failsafe Default Select DVMT5.0 Total Graphic Memory sized used by the Internal Graphics Device. VT- d Enabled Disabled...

Page 99: Peg Port Configuration

3.5.2 PE G Port Configuration Op tions Summary Max Link Speed Auto Optimal Default, Failsafe Default Gen 1 Gen 2 Gen 3 Configure PEG 0:1:0/0:1:1 Max Speed Chapter 3 – AMI BIOS Setup...

Page 100: Pch-Io Configuration

3.5 .3 PCH-IO Configuration Op tions Summary HD A udio Enabled Optimal Default, Failsafe Default Disabled Control the Detection of the Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled. PCI Express x4 Slot (x4) Auto Optimal Default, Failsafe Default P CI e Speed...

Page 101: Setup Submenu: Security

3.6 Se tup Submenu: Security Change User/Administrator Password Y ou can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Page 102: Secure Boot

3.6.1 Se cure Boot Op tions Summary Secure Boot Disable Optimal Default, Failsafe Default Enable Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System mode is in User mode. The mode change requires platform reset. Secure Boot Mode Standard Custom...

Page 103: Key Management

3.6.1.1 Ke y Management Op tions Summary Factory key Provision Disabled Optimal Default, Failsafe Default Enabled Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode. R estore Factory Keys Press 'Y es' to install factory default keys Y es Force System to User Mode.

Page 104

Secure Boot variable |Size | Keys#| key Source Platform key (PK) | Details Enroll Factory Defaults or load certificates from a 1153 | 1 | No Key file: 1.Public key Certificate: Export a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) Update d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable...

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Secure Boot variable |Size | Keys#| key Source Forbidden Details Enroll Factory Defaults or load certificates from a Signatures | 3274 | file: 77 | No Key 1.Public key Certificate: Export a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) Update c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX Append 2.Authenticated UEFI Variable...

Page 106: Setup Submenu: Boot

3.7 Se tup Submenu: Boot Op tions Summary Quiet Boot Disabled Enabled Optimal Default, Failsafe Default Enables or disables Quiet Boot option. Chapter 3 – AMI BIOS Setup...

Page 107: Setup Submenu: Save & Exit

3.8 Se tup Submenu: Save & Exit Chapter 3 – AMI BIOS Setup...

Page 108: Chapter 4 - Drivers Installation

Chapter 4 Chapter 4 – Drivers Installation...

Page 109: Drivers Download And Installation

Dri vers Download and Installation Drivers for the BOXER-6840-CFL can be downloaded from the product page on the AAEON website by following this link: https://www.aaeon.com/en/p/vision-system-box-pc-solutions-boxer-6840-cfl Download the driver(s) you need and follow the steps below to install them. I nstall Chipset Drivers Unzip the Chipset driver zip file Run the Set upChipset.exe file in the folder Follow the instructions...

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I nstall LAN Drivers Unzip the LAN driver zip file Run the P R OWinx64.exe file in the folder Follow the instructions Drivers will be installed automatically I nstall Audio Drivers Unzip the Audio driver zip file Run the 0008-64bit_Win7_Win8_Win81_Win10_R281.exe file in the folder Follow the instructions Drivers will be installed automatically I nstall Intel RST Drivers...

Page 111: Appendix A - Watchdog Timer Programming

Appendix A Appendix A - Watchdog Timer Programming...

Page 112: Watchdog Timer Introduction

Watchdog T imer Introduction This section details the initial program setting for the Watchdog Timer program. If you have any questions or need support, please contact an AAEON representative by visiting the support page at AAEON.com Please refer to the Linux Driver User Guide to access DIO, Watchdog Timer and Hardware Manager.

Page 113: Watchdog Timer Initial Program

A.2 Watchdog T imer Initial Program Tab le 1: Super IO relative register table Default Value N o te SIO MB PnP Mode Index Register Index 0x2E(Note1) 0x2E or 0x4E SIO MB PnP Mode Data Register Dat a 0x2F(Note2) 0x2F or 0x4F Tab le 2: Watchdog relative register table R egister B itNum...

Page 114

********** // SuperIO relative definition (Please reference to Table 1) #define byte SIOIndex //This parameter is represented from Note1 #define byte SIOData //This parameter is represented from Note2 #define void IOWriteByte(byte IOPort, byte Value); #define byte IOReadByte(byte IOPort); // Watch Dog relative definition (Please reference to Table 2) #define byte TimerLDN //This parameter is represented from Note3 #define byte TimerReg //This parameter is represented from Note4 #define byte TimerVal // This parameter is represented from Note24...

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********** Main VOID // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) // (boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure : AaeonWDTEnable // This procudure will enable the WDT counting. AaeonWDTEnable(); ********** Appendix A – Watchdog Timer Programming...

Page 116

********** // Procedure : AaeonWDTEnable AaeonWDTEnable () VOID WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1 // Procedure : AaeonWDTConfig AaeonWDTConfig () VOID // Disable WDT counting WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0 // Clear Watchdog Timeout Status WDTClearTimeoutStatus(); // WDT relative parameter setting WDTParameterSetting();...

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****

SIOEnterMBPnPMode() VOID IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); SIOExitMBPnPMode() VOID IOWriteByte(SIOIndex, 0xAA); SIOSelectLDN(byte LDN) VOID IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value) VOID Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(byte IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData); TmpValue &= ~(1 <<...

Page 118: Appendix B - I/O Information

Appendix B Appendix B - I/O Information...

Page 119: I/O Address Map

I/O Address Map Appendix B – I/O Informati o n...

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Appendix B – I/O Informati o n...

Page 121: Irq Mapping Chart

B.2 IRQ Mapping Chart Appendix B – I/O Informati o n...

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Appendix B – I/O Informati o n...

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Appendix B – I/O Informati o n...

Page 131: Memory Address Map

B.3 Me m or y Address Map Appendix B – I/O Informati o n...

Page 132: Appendix C - Digital I/O Ports

Appendix C Appendix C - Digital I/O Ports...

Page 133: Dio Introduction

DIO Introduction This section details the specifications and information needed to setup and program the Digital I/O ports for your system (DIO). Please refer to the Linux Driver User Guide to access DIO, Watchdog Timer and Hardware Manager. The User Guide is available to download from the Drivers section of the product page.

Page 134: Dio Programming

C.3 DIO Programming BOXER-6840-CFL utilizes FINTEK F81966 chipset as its Digital I/O controller. The following sections detail the procedures to complete its configuration. There are three steps to complete the configuration setup: St ep 1 Enter MB PnP Mode. St ep 2 Modify the data in the configuration registers.

Page 135: Digital I/O Register

C.4 Di gital I/O Register Tab le 1: SuperIO relative register table Default Value N o te SIO MB PnP Mode Index Register I nd ex 0x2E(Note1) 0x2E or 0x4E SIO MB PnP Mode Data Register Dat a 0x2F(Note2) 0x2F or 0x4F Tab le 2: Digital Input relative register table R egister B itNum...

Page 136: Digital I/O Sample Program

C.5 Di gital I/O Sample Program
********** // SuperIO relative definition (Please reference to Table 1) #d efine byte SIOIndex //This parameter is represented from N o te1 #d efine byte SIOData //This parameter is represented from N o te2 #d efine vo id IOWriteByte(b yte IOPort, b yte Value);...

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********** // Digital Output control relative definition (Please reference to Table 3) #d efine byte DOutput1LDN // This parameter is represented from N ote27 #d efine byte DOutput1Reg // This parameter is represented from N o te28 #d efine byte DOutput1Bit // This parameter is represented from N o te29 #d efine byte DOutput1Val // This parameter is represented from N o te30 #d efine byte DOutput2LDN // This parameter is represented from N ote31 #d efine byte DOutput2Reg // This parameter is represented from N o te32...

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********** VOID Main(){ Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read Digital I/O Pin 3 status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin level is High PinStatus = AaeonReadPinStatus(DI nput3LDN, DInput3Reg, DInput3Bit); // Procedure : AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...

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********** Boolean A aeonReadPinStatus(byte LDN, byte Register, byte BitNum){ Boolean PinStatus ; PinStatus = SIOBitRead(LDN, Register, BitNum); Return PinStatus ; VOID A aeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){ ConfigToOutputMode(LDN, Register, BitNum); SIOBitSet(LDN, Register, BitNum, Value);
********** Appendix C – Digital I/O Information...

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********** VOID SI OEnterMBPnPMode(){ IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87); VOID SI OExitMBPnPMode(){ IOWriteByte(SIOIndex, 0xAA); VOID SI OSelectLDN(byte LDN){ IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN); VOID SI OBitSet(byte LDN, byte Register, byte BitNum, byte Value){ Byte TmpValue; SIOEnterMBPnPMode();...

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********** Boolean SIOBitRead(byte LDN, byte Register, byte BitNum){ Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(LDN); IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData); TmpValue &= (1 << BitNum); SIOExitMBPnPMode(); If(TmpValue == 0) Return 0; Return 1; VOID Co nfigToOutputMode(byte LDN, byte Register, byte BitNum){ Byte TmpValue, OutputEnableReg; OutputEnableReg = Register-1;...

Page 142: Appendix D - Glue Removal Procedure

Appendix D Appendix D – Glue Removal Procedure...

Page 143: Removing Glue From Y Our System

Re m oving Glue f rom Your System To protect components from damage and ensure proper operation out of the box, glue may have been applied to some cables or connectors to keep them in place during shipping. This glue must be removed before attempting to swap components or perform maintenance.

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St ep 1: Using an eyedropper or bottle as shown above, apply a few drops of alcohol to the glue. St ep 2: Allow the alcohol to soak for 10 seconds, then use a cotton swab or cotton with anti-static tweezers to evenly rub the alcohol over the glue. St ep 3: Let soak for 10 more seconds, then use anti-static tweezers to remove the glue.

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If you encounter any issues or need support, please contact your AAEON representative or visit our Support Page at AAEON.com Appendix C – Digital I/O Information...