TOSHIBA

Toshiba TC9349AFG Manual

Cmos digital integrated circuit silicon monolithic

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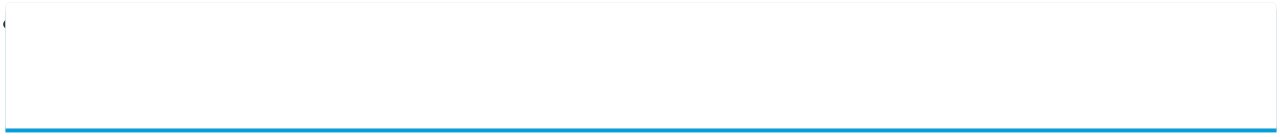

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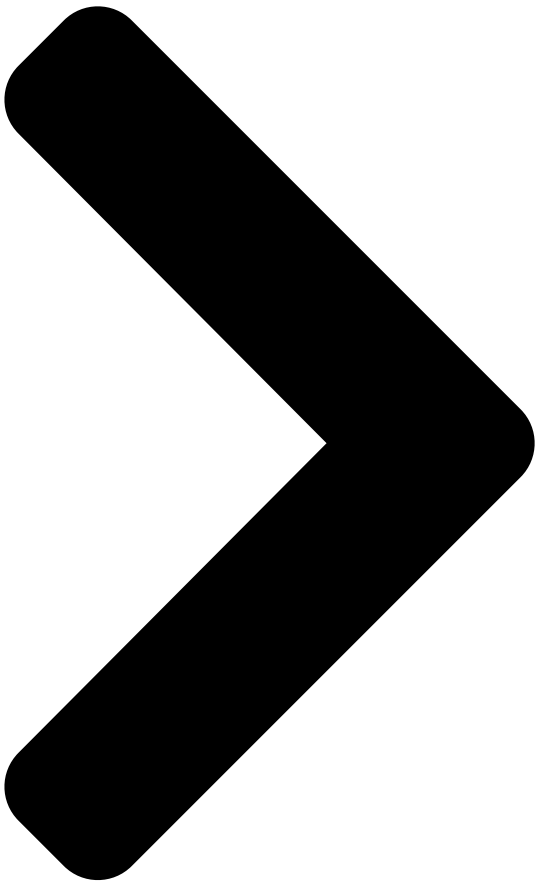


TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

Single-Chip DTS Microcontroller (DTS-21)

The TC9349AFG is a single-chip DTS microcontroller for portable audio incorporating a 30 MHz prescaler, PLL, and LCD driver. In addition to an IF counter, serial interface and buzzer function, the device incorporates an interrupt function, timer counter, pulse counter, electronic volume function and A/D converter

The device also supports selection of 1/4-duty 1/2 bias or 1/4-duty 1/3 bias for the LCD driver, while a built-in 3 V voltage doubler boosting circuit implements stable operation of the LCD monitor.

The power supply voltage ranges from 0.9 V to 1.8 V. Due to its low-current consumption, the device is suitable for use in digital tuning systems in portable equipment such as headphone stereos.

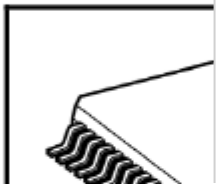
Features

•

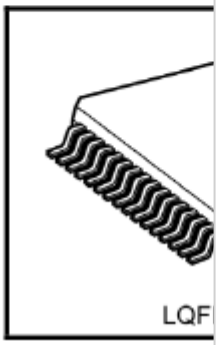
CMOS DTS microcontroller LSI with built-in prescaler PLL and LCD driver

•

Operating voltage range:



- Current dissipation:
- Operating temperature range:
- Program memory (ROM):
- Data memory (RAM):
- Oscillator frequency:
- Instruction execution time:
- Interrupt:
- Interrupt stack:
- Address stack:
- I/O port:
- LCD driver:
- Serial Interface:
- Buzzer:
- Timer counter:
- Pulse counter:
- Electronic volume:
- A/D converter:
- Amplifier for LPF:
- DC/DC converter of VT:



TC9349AFG

VDD = 0.9 to 1.8 V (typ.: 1.5 V)
With CPU in operation: IDD = 150 μA (typ.)
With PLL in operation: IDD = 1 mA (typ. At inputting OSCin = 30 MHz)
Ta = −10 to 60°C
16-bit × 8192 steps
4-bit × 512 words
Crystal oscillator:
75 kHz (crystal oscillator)
High-speed oscillator: 300 to 600 kHz (ceramic oscillator or crystal oscillator)
Crystal oscillator: 40 μs
High-speed oscillator: 5 to 10 μs
External: 2 system (INTR1, INTR2 pin)
Internal:
4 system (serial-interface, timer-port, timer-counter, decreased voltage detection)
4 level × 26 bit G-register, Data select, Carry flag, Data register
16 level × 13 bit (program counter)
CMOS I/O port: 36 (max)
N-ch open-drain I/O port: 9 (max)

Exclusive output port: 2 (max), exclusive input port: 1 (max)
1/4 duty, 1/2 bias or 1/4 duty, 1/3 bias: 28 segments (max)
1 system, 2 channel (N-ch open-drain, CMOS I/O port), 3 kinds (3-wired, 2-wired, UART)
4 kinds of frequency (1 kHz, 1.56 kHz, 2.08 kHz, 3 kHz),
4 modes (continuous, single-shot, 10 Hz intermittent, 10 Hz intermittent 1 Hz interval)
8 bit, 2 kinds of timer clock (25 kHz, 1 kHz),
2 modes (timer counter, pulse width measure (INTR1 pin))
8 bit up/down counter
2 channel, 32 step (0 dB to −78 dB, −∞dB)
6 bit, 4 channel, conversion time: 240 µs
5.5 V output max. (Tout, Tin)
2 stage (0.75 V, 1.0 V) voltage detected (VDET)
15 kinds of doubler clock, 2 types of doubler clock output
(CMOS output: DDCK2, N-ch output: DDCK1)

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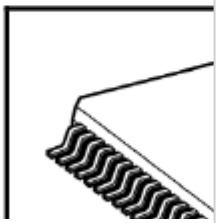
TC9349AFG

Weight: 0.32 g (typ.)

2006-02-24



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Related Manuals for Toshiba TC9349AFG

Microcontrollers Toshiba H1 Series Data Book

32bit micro controller tlcs-900/h1 series (751 pages)

Microcontrollers Toshiba TXZ Family Reference Manual

32-bit risc microcontroller txz family reference manual comparator (comp-b) (15 pages)

Microcontrollers Toshiba T6K04 Handbook

Cmos digital integrated circuit silicon monolithic column row driver lsi for a dot matrix graphic lcd (31 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (544 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (652 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Data Book

32bit micro controller (495 pages)

Microcontrollers Toshiba TLCS-900/H1 Series Manual

Original cmos 32-bit microcontroller (68 pages)

Microcontrollers TOSHIBA TXZ SERIES Reference Manual

Oscillation frequency detector (20 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller. can controller (can-a) (54 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller advanced encoder input circuit (32-bit) (55 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller, serial peripheral inteface tspi-b (67 pages)

Microcontrollers Toshiba TXZ Series Reference Manual

32-bit risc microcontroller (17 pages)

Microcontrollers TOSHIBA TXZ Reference Manual

32-bit risc microcontroller (120 pages)

Microcontrollers Toshiba TMP91C824F Data Book

16bit microcontroller tlcs-900/l1 series (255 pages)

Microcontrollers Toshiba TMP96C141AF Manual

Cmos 16-bit microcontroller (178 pages)

Microcontrollers Toshiba TC9314F Manual

Cmos digital integrated circuit silicon monolithic (66 pages)

Summary of Contents for Toshiba TC9349AFG

Page 1 TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic TC9349AFG Single-Chip DTS Microcontroller (DTS-21) The TC9349AFG is a single-chip DTS microcontroller for portable audio incorporating a 30 MHz prescaler, PLL, and LCD driver. In addition to an IF counter, serial interface and buzzer function, the device incorporates an...

Page 2 TC9349AFG • DC/DC converter for CPU: Charge-pump type Two kinds of doubler clock: 75 kHz crystal oscillator, high-speed oscillator clock (300 to 600 kHz), setting doubler voltage for 3 stages (2.0 V, 2.5 V, 3.0 V) • 16-bit HF mode: 1/15 or 16-pulse swallow-type (1 to 30 MHz,

Vin = 0.1Vp-p (min)) Programmable counter: LF mode: 12 bit direct divider type (0.5 to 4 MHz, Vin = 0.1Vp-p (min))

Page 3 TC9349AFG Pin Assignment Electronic volume SIO1 IFin/IN P15-1/S14 Pull-up/pull-down P15-0/S13 CMOS I/O port (34) OSCin P14-3/S12 GND (PLL) P14-2/S11 DO1/OT1/P P14-1/S10 DO2/OT2/N/Tin P14-0/S9 N-ch open drain P9-0/Tout P13-3/S8 I/O port (1) SVFP64 MUTE/P9-1 P13-2/S7 (0.5 mm pitch) CMOSI/O port (2)

Page 4 TC9349AFG Block Diagram P6-3/ADin4 (BRK12) MUTE R/WBuf. P6-2/ADin3 (BRK11) G-Reg. Port 6 P6-1/ADin4 (BRK10) MUTE P6-0/ADin4 (BRK9) (4 × 512 Words) P8-0/VDET (BRK13) Conv. P8-1/SI2/DDCK1 (BRK14) Port 8 P8-2/SCK2/RX2 (BRK15) Interrupt Stack Reg. P8-3/SDIO2/TX2 (BRK16) (4 Levels) DDCK1 VDET Data...

Page 5 TC9349AFG Description of Pin Functions PIN No. Symbol Pin Name Function and Operation Remarks out1 out1 Xin1 fXT1 Crystal oscillator pins. Crystal oscillator pin A reference 75 kHz crystal resonator is connected to the Xin1 and Xout1 pins. Xout1 out1...

Page 6 TC9349AFG PIN No. Symbol Pin Name Function and Operation Remarks Doubler output pin for the LCD driver. The VLCD pin doubles the VEE pin voltage to 3 V using the voltage doubler capacitance between C3 and C4. The doubled VLCD voltage is supplied to...

Page 7 TC9349AFG PIN No. Symbol Pin Name Function and Operation Remarks 22-bit CMOS I/O ports, allowing input and output to be programmed in 1-bit units. P10-0/COM1 I/O port 10 15 ~ 18 It can be set as LCD driver output through...

Page 8 TC9349AFG PIN No. Symbol Pin Name Function and Operation Remarks 4-bit CMOS I/O Port, allowing input and output to be programmed in 1-bit units. When the I/O port is set as input, the pull-up/pull-down state can be programmed in 1-bit units.

Page 9 TC9349AFG PIN No. Symbol Pin Name Function and Operation Remarks 8-bit CMOS I/O Port, allowing input and output to be programmed in 1-bit units. P4-0/INTR1 I/O port 4 When P4-0 to P4-3 ports are set as the (BRK5) /External interrupt...

Page 10 TC9349AFG PIN No. Symbol Pin Name Function and Operation Remarks IF signal input pin. The input frequency is between 0.03 and 12 MHz. A built-in input amp and C coupling allow small-amplitude operation. The IF counter can store 20-bit data in fin2 memory.

Page 11 TC9349AFG PIN No. Symbol Pin Name Function and Operation Remarks PLL phase comparator output pins. Tristate output: When the program counter divider output is higher than the reference frequency, High level is output; when the out1 output is lower, Low level; and when they match, high impedance.

Page 12 TC9349AFG PIN No. Symbol Pin Name Function and Operation Remarks The port 8 is a 4-bit N-ch open-drain I/O port, allowing control of ON/OFF for an output transistor to be programmed in 1-bit units When an output is set as OFF, the pin can be used as an input port.

Page 13 TC9349AFG Description of Operations The CPU consists of a program counter, a stack register, an ALU, program memory, data memory, a G-register, a data register, a DAL address register, a carry flip-flop (F/F), a judge circuit, interrupt stack register and an interrupt circuit.

Page 14 TC9349AFG 2. Address Stack Register (ASR) The address stack register consists of 16 × 14 bits. When the subroutine call instruction is executed or an interrupt is processed, this register stores a value equal to the contents of the program counter + 1 (that is, the return address).

Page 15 TC9349AFG 5. Data Memory (RAM) The data memory consisting of 4 bits × 512 words is used to store data. These 512 words are expressed in a row address (4 bits) and column address (4 bits). 348 words (row address = 04H to 1FH) within the data memory are addressed indirectly by the G-register.

Page 16 TC9349AFG 6. G-register (G-REG) The G-register is a 5-bit register used for addressing the row address (DR = 00H to 1FH) of the data memory’s 512 words. This register is located on the I/O map and accessed by input-and-output instruction. The 5-bit contents can be

directly set by execution of the STIG instruction.

Page 17 TC9349AFG 13. Instruction Set Table A total of 59 instruction sets are available, and all of these are single-word instructions. These instructions are expressed with a 6-bit instruction code. Upper 2 bits Lower 4 bits 0000 M, I TMTR r, M...

Page 18 TC9349AFG 14. Instruction Function and Operation Table (Description of the symbols used in the table) Data memory address Normally, an address within 000H to 03FH in the data memory. Data memory address (256 words) An address within 000H to 0FFH in the data memory.

Page 19 TC9349AFG Machine Language (16 Bits) Skip Mnemonic Function Operation Instruction Function (6 Bits) (2 Bits) (4 Bits) (4 Bits) Add immediate data M ← (M) + I M, I 000000 to memory Add immediate data M ← (M) + I + ca...

Page 20 TC9349AFG Machine Language (16 Bits) Skip Mnemonic Function Operation Instruction Function (6 Bits) (2 Bits) (4 Bits) (4 Bits) Load memory to r ← (M*) r, M* 0101 general register (4 bits) Store memory to M* ← (r) M*, r...

Page 21 TC9349AFG Machine Language (16 Bits) Instruction Skip Mnemonic Function Operation Function (6 Bits) (2 Bits) (4 Bits) (4 Bits) Test general register bits by Skip if r [N (M)] = all TMTR r, M memory bits, then 010000 “1” skip if all bits...

Page 22 TC9349AFG Machine Language (16 Bits) Instruction Skip Mnemonic Function Operation Function (6 Bits) (2 Bits) (4 Bits) (4 Bits) Shift memory bits to 0 → (M) b3 → (M) b2 → SHRC M right direction with 111111 0000 (M) b1 → (M) b0→ (CY) carry (M) b3 →...

Page 23 TC9349AFG I/O Map, Data Select Port (φL/K1A) All the ports within the device are expressed with a matrix of six I/O instructions (OUT1 to 3 instructions and IN1 to 3 instructions) and 4-bit code numbers. The allocation of these ports is shown on the following page in the form of an I/O map. The ports used in the execution of the various I/O instructions on the horizontal axis of the I/O map are allocated to the port code numbers indicated on the vertical axis.

Page 24 TC9349AFG Data port (φL10 to 16, φK10 to 11) on the I/O map is divided into 16 and indirectly specified by the contents of the data select port (φL/K1A). The indirectly specified port is accessed by the OUT1 instruction with the operand [CN = 0 to 6H] or IN1 instruction with the operand [CN = 0 to 1H].

Page 25 TC9349AFG I/O Map (IN1 (M, C), IN2 (M, C), IN3 (M, C), OUT1 (M, C), OUT2 (M, C), OUT3 (M, C)) φL1 φL2 φL3 φK1 φK2 φK3 Page 1 OUT1 OUT2 OUT3 Data port 1 Interrupt enable flag Data port 1...

Page 26 TC9349AFG φL/K1A Data select SEL1 SEL2 SEL4 SEL8 φL10 φK10 φL11 φK11 OUT1 OUT1 φL/K1A Address stack pointer (ASP) Address stack pointer (ASP) DAL address 1 (AR) DAL address 1 (AR) ASP0 ASP1 ASP2 ASP3 ASP0 ASP1 ASP2 ASP3 Address stack select...

Page 27 TC9349AFG φL/K1A Data select φL12 φL13 φL14 φL15 φL16 OUT1 OUT1 OUT1 OUT1 OUT1 φL/K1A I/O port 9 output data Buzzer output control 1 IF counter control 1 Prescaller COM1 COM2 COM3 COM4 IFin I/O port 10 output data Buzzer output control 2...

Page 28 TC9349AFG System Reset The device system will be reset when the RESET pin is subject to the “L” level or when a voltage of 0 V → 1.2 V to 3.6 V is supplied to the V pin (power-on reset). On system reset, the program will start from “0” address immediately after a standby time of 100 ms following the startup of the low-speed oscillator.

Page 29 TC9349AFG System clock control circuit The system clock control circuit consists of a clock generator, clock generator control port, timing generator and backup mode control circuit. Clock generator Clock generator Backup mode control port control circuit OUT1 φ L15F)

Page 30 TC9349AFG 2. Clock generator control port The clock generator control port controls the low-speed and high-speed oscillators. OSC2 φL15(F) INV ON 0: Low-speed oscillator Selection of CPU clock 1: High-speed oscillator 0: Oscillator stop High-speed oscillator 1: Oscillator control 0: Constant-current system...

Page 31 TC9349AFG DC/DC converter for CPU The device incorporates a DC/DC converter for the CPU power supply. The CPU doubler circuit comprises a charge pump system utilizing a capacitor. There is a built-in clamp control function, for which an electrical potential of 2.0, 2.5 and 3.0 V can be set through programming.

Page 32 TC9349AFG Doubler clock CLAMP Doubler circuit Internal reference voltage Internal doubler voltage (A/D converter, constant- voltage V DD V DB circuit) Doubler voltage Example of an Application Circuit for a Charge Pump Doubler System Utilizing a Capacitor Note: The V pin is fixed at the V pin level while the clock stop instruction is being executed.

Page 33 TC9349AFG Constant-voltage circuit (V There is a built-in constant-voltage circuit (V) to provide the reference voltage of the LCD driver and DC/DC converter for the VT and for the CPU and A/D converter. The constant-voltage circuit utilizes the doubler V pin power supply for the CPU and outputs a constant voltage of 1.5 V from the V...

Page 34 TC9349AFG Backup mode Backup mode decreases the operating current and holds data memory and other registers. Backup mode can be implemented through programming-based backup or hardware-based backup. For programming-based backup, three types of backup mode are possible through the executing of CKSTP or WAIT instructions.

Page 35 TC9349AFG When a voltage of approx. 0.5 V or more is impressed, it is released. OUT1 Clock stop Standby Clock stop (backup) (about 100 ms) operation operation CKSTP pin Executing of Executing of CKSTP instruction CKSTP instruction Example for Operating Timing by Power Supply Pin...

Page 36 TC9349AFG HARD WAIT mode The operations of all elements, with the exception of the crystal resonator and doubler operating (V pin), can be suspended by execution of a WAIT instruction in which [P = 1H] has been specified in the operand. This enables even greater levels of current consumption reduction than SOFT WAIT mode.

Page 37 TC9349AFG Detected power supply OFF function Detected power supply OFF function detects the fact that the power supply is off during battery exchange or similar procedures and actuates the backup state of the CPU circuit (V pin) to keep it on hold.

Page 38 TC9349AFG φL11(F) (decreased voltage control 2) STOP INT LB BREAK Reset Power supplies off break enable/power off function enable 0: Prohibition Function stop 1: Enable Function operation (Note) If not using this function, set this bit to "0" for consumption current reduction.

Page 39 TC9349AFG φL16(D) Decreased voltage TR3 TR2 TR1 TR0 Data (HEX) detection voltage (V) φK11(D) 0.850 Decreased voltage 0.875 detection setting data 0.900 Note: Decreased voltage detection voltage detected pin level. 0.925 Note: Any fall below decreased voltage 0.950 detection voltage will cause the STOP F/F to be set to "1";...

Page 40 TC9349AFG Backup circuit RESET Reset input C2 V 0.47 µ F POWER Schottky diode Example Capacitor Backup Circuit (1) RESET Reset input C2 V Schottky diode 0.47 µ F Release signal POWER input Example Battery Backup Circuit (2) Note: If backup operation using a CKSTP/WAIT instruction is available, use release signal input to perform the release operation as necessary.

Page 41 TC9349AFG PLL OFF mode The PLL can be turned on or off depending on the contents of the reference selection port. If all the contents of the reference selection port are set to "1", PLL off mode applies. (Refer to the section on the reference frequency divider.) When the ENA bit is set to "1", the PLL can be turned on or off with the...

Page 42 TC9349AFG Register port The G-register, data register and DAL address register, which were mentioned in the description of the CPU, are arranged on the I/O map, and treated as one of the internal ports. The carry flag can also be accessed from an I/O map. (Refer to the section on I/O access of the stack register.)

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TC9349AFG 2. Data register (φL/K1C ~ φL/K1F), DAL address register (φL/K11(0) ~ φL/K11(3)) and control bit The data register is 16-bit register for which the program memory data is loaded when the DAL instruction and DALR instruction are executed. The contents of this register are

loaded into the data memory in 4-bit units with the execution of the OUT1/IN1 instructions for which [CN = CH ~ FH] has been specified in the operand.

Page 44: Y1 Y2 Y4 Y8

TC9349AFG The DAL address register (AR) is a register that specifies the program-memory-indirect when the DALR instruction is executed with the 16-bit register. There are two types of commands that load the program memory data: the DAL instruction and the DALR instruction.

Page 45: Y2 Y4 Y8

TC9349AFG Stack register The stack register consists of an address stack register (ASR) and an interruption stack register (ISR). A stack register is used when subroutine call instructions and interrupt processing are executed. Interrupt stack registers comprise 26 G- register, data select, carry flag, and data register bits, as described in the register port item and I/O map. These stack registers are arranged on an I/O map, and are read from and written into with input and output instructions.

Page 46: Isrd8 Isrd9

TC9349AFG 2. Interrupt stack register (ISR) The interrupt stack register (ISR) is a 14 bit × 16 page register. When interrupt processing is executed, the contents of the 26-bit G-register, data selection, carry flag, and data register are stored automatically. This register consists of four pages and is specified with a two-bit interrupt stack pointer (ISP).

Page 47 TC9349AFG 3. I/O access of a stack register The stack register is arranged in the I/O map. Therefore reading the state of the stack register and rewriting data are possible. The contents of an address stack pointer (ASP) or an interruption stack pointer (ISP) can also be accessed. These data are accessed with an OUT1/IN1 instruction for which [CN = 0H] is specified for the operand, and divided and arranged by the data selection function.

Page 48 TC9349AFG Interrupt function There are six types of peripheral hardware for which the interrupt function can be utilized: the INTR1 terminal, the INTR2 terminal, the timer port, the serial interface, the timer counter, and the decreased voltage detection circuit. This peripheral hardware will issue an interrupt request signal if certain conditions are satisfied. On reception of an interrupt, the data for the G-register, data selection, carry flag, and data register are shunted to an interrupt stack register, and the return address is shunted to the address stack register.

Page 49 TC9349AFG Interrupt latch The interrupt latch is set to “1” through the issuing of an interrupt request from peripheral hardware. If interrupt is enabled, an interrupt reception request will be sent to the CPU, which will execute the interrupt routine and carry out branching.

Page 50 TC9349AFG Change of interrupt factor From among the ID numbers, ID Nos. 1 and 2 can be used to select, respectively, INTR2 pin / timer port and serial interface / timer port / decreased voltage detection. These changes are made through the control port in each block.

Page 51 TC9349AFG 2. Interrupt Reception Processing The interrupt request is held until interruption is received, it interrupts by system reset operation or the program and it resets a latch to "0" through programming. Interrupt reception operation is as shown below. 1) Each item of peripheral hardware outputs each interrupt request and sets the interrupt latch to “1” if the interrupt conditions are fulfilled.

Page 52 TC9349AFG 3. Return Processing from the Interrupt Processing Routine The only RNI instruction is used to return the operational state to the processing being carried out before reception of the interrupt from the interrupt routine. Execution of the RNI instruction causes the following processing to be carried out automatically in sequence.

Page 53 TC9349AFG Exercise particular care regarding the following points when using multiplex interrupt: The priority of the interrupt factors Restrictions on the address stack levels used when interrupt requests are issued. Shunting processing for the carry flag, data memory, etc. Priority of interrupt factor The order of priority for multiplex interrupt becomes A <...

Page 54 TC9349AFG External Interrupt and Timer Counter Functions There are two types of pin for external interrupt: INTR1 and INTR2. An interrupt request is issued on detection of the edge of the signal applied to pins INTR1 and INTR2, whether rising, falling or both. The interrupt

input pins also combine the functions of I/O port;...

Page 55 TC9349AFG 2. Timer Counter Function The timer counter consists of an 8-bit binary counter, a counter coincidence register, a digital comparator, and a control circuit for controlling these items. The timer counter function has a timer mode and a pulse width measurement mode.

Page 56 TC9349AFG Timer mode Timer mode is a mode for detecting a regular time. Whenever the regular time is detected, an interrupt request is executed and the counter reset. At this time, the control bit is set to 25 kHz or 1 kHz, the PW bit to “0”, and the CR bit to “0”.

Page 57 TC9349AFG INTR1 input Timer clock Timer counter data 01H 02H ID(n-1) ID(n+1) ID(n+2) Coincidence pulse Interrupt is issued if counter data and When the counter data is corresponding to the agreement coincidence data correspond Counter reset pulse data, it issues it interrupt.

Page 58 TC9349AFG Internal Interrupts and the Interrupt Function There are four types of internal interrupt: timer port, timer counter, serial interface, and decreased voltage detection. Of these, three types of interrupt: timer port; serial interface; and decreased voltage detection; can serve a double purpose and act as interrupts for other factors.

Page 59 TC9349AFG Timer port Equipped with 200 Hz, 100 Hz, 10 Hz and 2 Hz F/F bits, the timer is used for counting of clock operations and of tuning scan mode. Through selection in the timer port for interrupt, interrupts can be generated with a 100 Hz or 200 Hz rising edge.

Page 60 TC9349AFG The 10 Hz, 100 Hz and 200 Hz timer is output to 10 Hz, 100 Hz and 200 Hz bits respectively with frequency pulses of 100 ms, 10 ms and 5 ms respectively. The 10 Hz and 100 Hz timers have a duty cycle of 50%. The 200 Hz timer is output at a duty cycle of 60% with a high level of 3 ms and a low level of 2 ms.

Page 61 TC9349AFG Input and Output Ports A maximum of 45 I/O ports are available for the input/output of control signals. These 45 I/O ports include 36 CMOS I/O ports and 9 N-ch open-drain I/O ports. Up to one exclusive input ports and two exclusive output ports are also available.

Page 62 TC9349AFG I/O port 3 is a CMOS I/O port. Pins P3-0 to P3-2 are also used as the serial interface and pin P3-3 is also used as a pulse counter input pin. These pins can be set to pull-up or pull-down state and to the break function.

Page 63 TC9349AFG Control Ports of Input and Output Ports SEL1 SEL2 SEL4 SEL8 φL12(Data port 1) Data select OUT3 instruction IN3 instruction φL30 φK30 I/O port 9 output data φL31 φK31 I/O port 10 output data φL32 φK32 I/O port 11 output data...

Page 64 TC9349AFG I/O port input/output settings are determined at the I/O control data ports. Set the I/O control data port bit corresponding to each port to “0” to program as an input port or set to “1” to program as an output port.

Page 65 TC9349AFG 3. Break Setting and Pull-up/Pull-down Setting 16 pins of I/O ports 3, 4, 6 and 8 can be set as backup release pins (break pins). If there is a change in the input state of an I/O port that has been set to input, the break pin releases execution of the WAIT or CKSTP instruction and restarts the CPU operation.

Page 66 TC9349AFG Pull-up and pull-down settings can be used to configure the key matrix. The key matrix is configured with usual I/O port output as the output of the key matrix and the I/O port 3 that has been set to pull-down or pull-up as the key input. Setting the key input to break enables restarting depending on the presence or absence of this key input when the CDSTP or WAIT instruction is executed.

Page 67 TC9349AFG MUTE Output This is the 1-bit CMOS output port for muting control and also used as P9-1 of the I/O port. The MUTE output can be reversed by the output logic setting or changes in the I/O port. 1. MUTE Port MUTE φL/K28...

Page 68 TC9349AFG Serial Interface This is the 2-channel, 1-system serial interface, which has three functions; a three-wire serial interface, two-wire serial interface and full-duplex UART

functions. The serial interface communicates with the extended LSI and microcomputer using CMOS serial interface pins SCK1/TX1 (P3-0), SDIO1 (P3-1) and SI1 (P3-2) or N-ch open-drain pins SCK2/TX2 (P8-2), SDIO2 (P8-3) and SI2 (P8-1) (that can accept voltage up to 5.5V).

Page 69 TC9349AFG Serial interface control 2 シリアルインタフェースコントロール 2 Y 1 Y 2 Y 4 Y 8 φL11(8) OSC0 OSC1 Clock setting クロック設定 シリアルクロック(転送レート)周波数設定 Serial clock (transmission rate) frequency setting 2/3線式設定時 2/3-wired interface clock Oscillator OSC1 OSC0 発振器の設定 UART送受信転送レート(fSCK) UART transmission rate (fSCK) クロック周波数(fSCK)

Page 70 TC9349AFG Serial interface control 4 シリアルインタフェースコントロール 4 Y 1 Y 2 Y 4 Y 8 φL11(A) STPS SWENA 0: SDIO端子入力設定 0: Pin SDIO input setting SDIO端子シリアル出力の出力設定 Output setting for serial 1: SDIO端子出力設定 1: Pin SDIO output setting output of pin SDIO 0: ...

Page 71 TC9349AFG φL11(4) φL11(5) φL11(6) Y 1 Y 2 Y 4 Y 8 Y 1 Y 2 Y 4 Y 8 Y 1 Y 2 Y 4 Y 8 0: シリアル出力" " L シリアル出力データ セットしたデータが 出力カウンタ番号に対応した出力、 Serial output data Data that has been set outputs the output data 0: Serial output “L”...

Page 72 TC9349AFG Serial interface monitor 1 シリアルインタフェースモニタ 1 Y 1 Y 2 Y 4 Y 8 φK11(7) 0: 2 線式停止状態 BUSY1 SOERR RX F/F BUSY2 0: 2-wired stop state 2 線式設定時: 2 線式動作状態の検出 2-wired mode: Detection of 1: 2 線式動作状態 1: 2-wired operating...

Page 73 TC9349AFG 1-1. Serial Interface Setting and Control Bits Serial pin setting (PSEL and SIO bits) I/O ports 3 or 8 can be used as serial input/output pins. I/O port 3 has a CMOS structure and I/O port 8 has an N-ch open drain structure.

Page 74 TC9349AFG シリアルクロック(転送レート)周波数設定 Serial clock (transmission rate) frequency setting 2- or 3-wired interface clock 2/3線式設定時 Oscillator OSC1 OSC0 発振器の設定 UART送受信転送レート(fSCK) UART transmission rate (fSCK) frequency (fSCK) クロック周波数(fSCK) setting fosc/2 37.5kHz Low-speed fosc/4 18.75kHz fosc/8bps 9375bps 9600bpsモード mode 低速発振器 oscillator (75kHz) (75kHz) fosc/8 9.375kHz...

Page 75 TC9349AFG POL bit (Selection of serial clock logic for serial data) Select the logic for shift clock input/output of the serial clock. When "1" is set to the bit of POL and a master setup is selected, serial operation stops on the "H" level in the state of a stop, if operation starts, the serial clock outputs and it stops on "H"...

Page 76 TC9349AFG NchS bit (Selection of output form for the serial I/O port pins) Set the serial interface input/output circuit type. Setting this bit to “0” to select the CMOS circuit form, and setting this bit to “1” to select the N-ch open-drain circuit.

Page 77 TC9349AFG STPS bit (Selection of the serial clock counter stop condition) The serial operation stops when it becomes the stop position of a serial counter. There are two types of serial counters, the serial output counter and the serial input counter. The stop condition is switched between the output and input counters.

Page 78 TC9349AFG SOS bit (Output setting for SDIO pin serial output) This control bit switches the serial data input/output pin (SDIO pin) between data output and input. Set this bit to “0” for serial data input or set to “1” for serial data output.

Page 79 TC9349AFG MSB bit (Selection of the order of serial data bits) This control bit controls the arrangement of serial data input/output data. Select whether data input/output started from the most or the least significant bit respectively. For the serial interface, serial data specified by the serial counter is inputted and outputted. The MSB bit controls the serial counter to count up or down.

Page 80 TC9349AFG Serial counter, Serial data (STA0 to 3, STP0 to 3, OCT0 to 3 and ICT0 to 3 bits, SO0 to SO9/SOE/SOF, SI0~SI9/SIE/SIF) The serial counter consists of the serial input counter (ICT0 to 3) that counts the serial input clock and the serial output counter (OCT0 to 3) that counts the serial output clock.

Page 81 TC9349AFG Start and stoppage of serial operation TSTA1 and TATA2 bits (Start of serial operation) The TSTA1 bit controls the start of serial operation in the master mode. When this bit is set to “1”, the serial clock will be outputted and the serial interface operation will

start.

Page 82 TC9349AFG Serial operation monitor BUSY1/BUSY2 bits (Operation monitor) The BUSY1/BUSY2 bits detect the serial operating state. The BUSY1 bit can detect the serial clock operating state, while the BUSY2 bit can detect the operating state in the 2-wire mode or the receiving operation state in the UART mode.

Page 83 TC9349AFG 1-2. Examples of Serial Mode Settings Examples of settings in the 3-wire, 2-wire and UART modes are shown below. Adjust settings according to the required specifications. Example of 3-wire serial mode setting Setting bit Condition setting data 3-wire setting (M0 = 0, M1 = 1)

Page 84 TC9349AFG Example of serial mode setting in the 2-wire mode Setting bit Condition setting data 2-wire setting (M0 = 0, M1 = 1) M0, M1 CK0, CK1, OSC0, OSC1 Serial clock frequency setting Master setting (MASTER = 1): Refer to an example of master operation timing.

Page 85 TC9349AFG Example of UART mode setting Setting bit Condition setting data UART setting (M0 = 0, M1 = 1) M0, M1 CK0, CK1, OSC0, OSC1 Transmission rate setting Master setting (MASTER = 0) MASTER Serial clock stop state = H ...

Page 86 TC9349AFG 1-3. Serial Clock Timing Serial clock シリアルクロック (SCK) （ SCK) シリアル出力 Serial output （ SDIO) (SDIO) TpLH TpHL シリアルクロック Serial clock （ SCK) (SCK) シリアル出力 Serial output （ SDIO) (SDIO) TpLH TpHL ・最小パルス幅 TpL/TpH) 2.5μs最小（: Minimum pulse width (TpL/TpH):2.5μs (minimum) ・伝達遅延時間(TpLH/TpHL) 50ns標準...

Page 87 TC9349AFG Pulse Counter The pulse counter is the 8-bit up/down counter that can detect the clock number through the CMOS input from PCTRin (P3-3) pin. It can be used for counting and detection of tape running. 1. Pulse counter control ports and data ports パルスカウンタコントロール...

Page 88 TC9349AFG The pulse counter measures the number of pulses of the input of PCTR in the (P3-3) pin. The POS and NEG bits specify the input pin clock edge from the rising edge, the falling edges and both edges. This bit is fixed in the normal operation.

Page 89 TC9349AFG Buzzer Output Buzzer output can be used for emitting beeps for acknowledgement and alarm purposes during key operations and when in tuning scan mode. The type of buzzer can be selected from combinations of four output modes and eight frequencies.

Page 90 TC9349AFG The buzzer output is also used as the P4-2 I/O port. It can be switched to buzzer output by setting the BUZR ON bit to “1” and setting the P4-2 I/O control port to output. Once the buzzer frequency, mode and logic are specified, set the buzzer enable bit to “1”, and the buzzer will be emitted.

Page 91 TC9349AFG Buzzer Output Timing ブザー周波数 Buzzer frequency "1" "0" "1" Data set to BEN bit ＢＥＮビットへのデータセット ブザー出力(モードA) Buzzer output (Mode A) BUZR 10H ｚ最大10ms BUZR 10 Hz 10 ms max. ブザー出力中にB Nビットに"1"を再度セットすると50ms延長される Ｅ。 Extended by 50 ms by setting the BEN bit again to “1”...

Page 92 TC9349AFG LCD Driver The LCD driver is also used as an I/O port, and it allows a maximum of 72 segments to turn on. When the LCD driver is enabled, I/O port 10 is switched to COM1 to COM4 pins and I/O port 12 is switched to S1 to S4 pins. Each of the 14 pins of I/O ports 13, 14, 15 and 16 can be set to segment pin output.

Page 93 TC9349AFG The LCD driver control ports are assigned to data control ports 4 and 5; as selected at the select port. These ports are accessed by using the OUT1 instruction with [CN = 3H, 4H] specified in the operand. LCD driver segment data The LCD driver segment data is specified at data ports 4 and 5 (φL13 and φL14).

Page 94 TC9349AFG 2. LCD Driver Configuration High-speed I/Oポート10 I/Oポート12 16 ～高速発振器 I/O port 10 I/O port 12 to 16 oscillator 定 VLCD 電ｋＨｚ Segment driver VLCD昇圧回路 セグメントドライバ圧 doubler Common 回 DISP OFF コモン出力回路 circuit output circuit 路セグメントデータ...

Page 95 TC9349AFG 3. LCD Driver Operation Timing LCD output waveform in the 1/2 bias mode (BIAS bit= “0”) In the 1/2 bias mode, the potential of the LCD driver waveform is outputted as V and GND and the V level is outputted at a frame frequency of 62.5 Hz.

Page 96 TC9349AFG LCD output waveform in the 1/3 bias mode (BIAS bit= “1”) The potential of the LCD driver waveform is outputted as V and GND, and the intermediate potential levels, 1/3 and 2/3 of potential V are outputted at a frame frequency of 125 Hz.

Page 97 TC9349AFG A/D Converter The A/D converter has four channels with 6-bit resolution, and can be used for measuring electrical field strength, measurements of battery and cell voltages and key input using ladder resistance. 1. A/D Converter Control Port and Data Port φL23...

Page 98 TC9349AFG 2. A/D Converter Circuit Configuration ADin1 (P6-0) Comparator Sample hold ADin2 (P6-1) SEL0~2 ADin3 (P6-2) BUSY ADin4 (P6-3) Control circuit STA BUSY doubled voltage) V EE constant-voltage circuit BUSY The A/D converter consists of a 6-bit D/A converter, a sample hold, a comparator, an A/D conversion latch and a control circuit.

Page 99 TC9349AFG Programmable Counter The programmable counter consists of a 2-modulus pre-scalar, a 4-bit and 12-bit programmable counter and a port that controls these elements. The programmable counter stops operation in the PLL off mode, and operates in the PLL on mode respectively. The radiation and consumption current can be reduced when the programmable counter is used in combination with the 1-chip tuner with a built-in 1/16 pre-scaler.

Page 100 TC9349AFG 2. Setting the Frequency Dividing Method and Gain of The Programmable Counter Using the HF bit, select the pulse swallow or direct frequency division methods; depending on the received frequency. The programmable counter is used in combination with the 1-chip tuner with a built-in 1/16 or 1/8 pre-scaler. Usually, use the tuner to input the local oscillation frequency, which is then inputted to the OSCin input in the MW/LW/SW wavebands.

Page 101 TC9349AFG Programmable Counter Circuit Configuration The circuit consists of an amplifier, 1/15□16 2-modulus pre-scaler, a 4-bit swallow counter and a 12-bit binary programmable counter. When the HF mode is selected, the 1/15□16 pre-scaler, the 4-bit swallow counter and the 12-bit binary programmable counter are used.

Page 102 TC9349AFG Reference Frequency Divider The external 75 kHz crystal oscillation frequency is divided to generate the following ten types of PLL reference frequency signals; 1 kHz, 1.39 kHz, 1.56 kHz, 2.78 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz and 25 kHz respectively.

Page 103 TC9349AFG Phase Comparator and Lock Detection port The phase comparator compares the reference frequency supplied from the reference frequency divider and the programmable counter divided frequency output to determine the phase difference and outputs errors. It then controls the voltage control oscillator (VCO) through the low-pass filter to match the frequency and phase difference of these two signals.

Page 104 TC9349AFG UNLOCK φL27 RESET □ 0 □□ 0: Off □□LPF□□ Built-in LPF control □ 1 □□ 1: On □ 0 □□□ 0: Positive logic Selection of PN output logic PN□□□□□□ □ 1 □□□ 1: Negative logic 0: Prohibition □ 0 □□...

Page 105 TC9349AFG Automatic phase difference switching mode (DO2 control 2 port: AUTO, ENA, CK0 and CK1 bits) The DO2 pin has an automatic phase difference switching mode that switches the output resistance automatically; depending on the phase difference. In this mode, the output resistance becomes higher as the phase difference pulse becomes shorter, and vice versa.

Page 106 TC9349AFG PN output mode (PN and POL bits) The PN output mode is available using an external charge pump. When this mode is selected, the two DO1/2 pins are switched to the P- and N-output pins. The P/N output logic can be reversed by using the POL bit.

Page 107 TC9349AFG Unlock detection port (UNLOCK RESET, UNLOCK F/F and ENA bits) The unlock F/F detects the phase difference between the programmable counter frequency-divided

output and the reference frequency at the timing with a phase shift of about 180°. If the phases do not match, or are in an unlocked state, the unlock F/F will be set.

Page 108 TC9349AFG 3. Phase Comparator and Unlock Port Circuit Configuration ~ Reference frequency 基準周波数 Phase 位相比較器 DO1/OT1/P comparator Programmable counter プログラマブル output カウンタ出力 R0,R1 PN POLビット、 PN and POL bits UNLOCK UNLOCK ENABLE UNLOCK RESET DO2/OT2/N/TIN Phase difference Programmable 位相差カウンタ...

Page 109 TC9349AFG DC-DC Converter for VT This product incorporates the DC-DC converter for the PLL low-pass filter. The DC-DC converter increases voltage by using coil induced electric power. There are two methods for increasing voltage; using the built-in N-channel transistor and using the external transistor. Select either method depending on the voltage to be increased.

Page 110 TC9349AFG Control 3 for DC-DC converter for VT VT 用 DC-DC コンバータコントロール 3 DDCK DDCK φL15(7) 0: Negative logic “H” or “HZ” output when the output is 0: 負論理...出力停止時“H”または“HZ”出力 Clock output logic setting クロック出力論理設定 stopped 1: 正論理...出力停止時“L”出力 1: Positive logic “L” output when the output is stopped 0: Prohibition (I/O port function) 0: 禁止...

Page 111 TC9349AFG 2. Setting of DC-DC Converter for VT Example of using the DDCK1 internal doubler transistor The DDCK1 pin includes an N-ch transistor for the DC-DC converter, and it can drive the coil directly. This transistor can withstand 6 V and no voltage over this level is permitted. Usually, the doubler clamp function is used to keep the limit the voltage.

Page 112 TC9349AFG Example of using the DDCK2 external doubler transistor The DDCK2 pin outputs the DC-DC converter clock in the CMOS type. The external transistor is used to increase the voltage like the DDCK1 pin. The doubled voltage can be set freely by using the external transistor. When the DDCK2 pin is used, set the POL bit to “1”.

Page 113 TC9349AFG 3. Configuration of DC-DC Converter for VT VLCD P9-2出力データ P9-2 output data ~ 75kHz DDCK2 PCTRin(P3-3) Counter カウンタ fXT2(高速発振器) fXT2 (high-speed oscillator) Counter カウンタ OSCin(fosc) DDCK ENA･DDCK SEL DD0 DD3 ~ VDET ENA VDET 0.75V 1.00V VDET ENA VDET SEL VLCD DDCK ENA･DDCK SEL...

Page 114 TC9349AFG Electronic Volume This product incorporates 2-channel 32-step (0 to −78 dB, −∞ dB) electronic volume. This allows digitization of volume control of headphone amplifier and reduction of parts. The electronic volume pins are also used as I/O port 5 and I/O port pin P4-3. Channels can be switched between channels 1 and 2, which support monaural and stereo sound.

Page 115 TC9349AFG Electronic volume control 電子ボリュームコントロール φL15(4) -∞dB MUTE 0: Normal operation (Electronic volume data attenuation) 0 通常動作 電子ボリュームデータ減衰量： () -∞dBビット - ∞ dB bit 1: - ∞ dB (Mute)： 1 -∞dB(ミュート) 0:禁止 0: prohibition Permission of - ∞ dB bit MUTEビットによる-∞dBビット制御許可...

Page 116 TC9349AFG 2. Electronic Volume Configuration and Circuit Example The electronic volume is configured by connecting the tuner and headphone amplifier as shown below. ~ VRout1 チューナ Tuner ~ VRin1 R channel output Rチャネル出力 Lチャネル出力 L channel output VRcom ~~...

Page 117 TC9349AFG 3. Electronic Volume Configuration The electronic volume is composed of a decoder, analog switches and resistors and the control circuit. The decoder, analog switches and resistors are powered by the V pin (3 V) power supply, which allows stable operation, even if the pin power supply fluctuates.

Page 118 TC9349AFG IF Counter This is a 20-bit general-purpose counter that counts the intermediate frequency (IF) of FM or AM during auto tuning and can be used to detect auto stop signals. It can also measure the VCO of the analog tuner and detect the received frequency.

Page 119 TC9349AFG IF monitor φ K17 BUSY OVER MANUAL 0: IF counter measured value < = 2 − 1 Overflow detection 1: IF counter measured value > = 2 (overflow state) 0: IF counter automatic mode Operation mode 1: IF counter manual mode...

Page 120 TC9349AFG 5. IF Counter Configuration The IF counter is composed of an input amplifier, a gate time control circuit and a 20-bit binary counter. The OSCin prescaler clock can

be inputted as the IF counter input. TA2/3 Prescaler IN IFin...

Page 121 TC9349AFG Test Port This is the internal port used to test the device functions. These ports are assigned to data port 7 and can be accessed by using the OUT1 instruction with [CN = 6H] specified in the operand. Set all to “0” in the normal program.

Page 122 TC9349AFG (Ta = 25°C) Absolute Maximum Rating Characteristics Symbol Rating Unit −0.3 ~ 4.0 Supply voltage (Note 1) −0.3 ~ V + 0.3 Output withstand voltage 1 (Note 2) −0.3 ~ 6.0 Output withstand voltage 2 (Note 2) −0.3 ~ V + 0.3...

Page 123 TC9349AFG (Unless otherwise specified, Ta = 25°C, V = 1.5 V, VDB Electrical Characteristics =3.0 V) Test Characteristics Symbol Test Condition Typ. Unit Circuit Operating supply voltage range (Note 1)) PLL operation Memory retention voltage range) Backup mode 0.75...

Page 124 TC9349AFG Constant Voltage Output (V), Voltage Doubled Output (V Test Characteristics Symbol Test Condition Typ. Unit Circuit) GND reference × Clamp off, Charge pump voltage) GND reference Clamp voltage = 2.0 V setting...

Page 125 TC9349AFG I/O Ports 1 to 6 (P1-0 to P16-3) , Serial Interface (SCK1/2, RX1/2, SDIO1/2, TX1/2) (Note 4) Test Characteristics Symbol Test Condition Typ. Unit Circuit = 0.9 V, V = 3.0 V, − 0.2 V −0.4 −0.8 ...

Page 126 TC9349AFG Electronic Volume (VRout1, VRin1, VRcom, VRin2, VRout2) Test Characteristics Symbol Test Condition Typ. Unit Circuit k Ω Volume resistance IN ~ GND resistor Ω Analog switch ON resistance Analog switch on resistor Δ ATT ...

Page 127 TC9349AFG DC-DC Converter Voltage Doubler for VT (VDET, DDCK1, DDCK2) Test Characteristics Symbol Test Condition Typ. Unit Circuit Doubled voltage range Doubled voltage detection setting Δ V) V EE = 1.5 V ± 0.05 error ...

Page 128 TC9349AFG Package Dimensions Weight: 0.32 g (standard) 2006-02-24...

Page 129 TC9349AFG 2006-02-24...