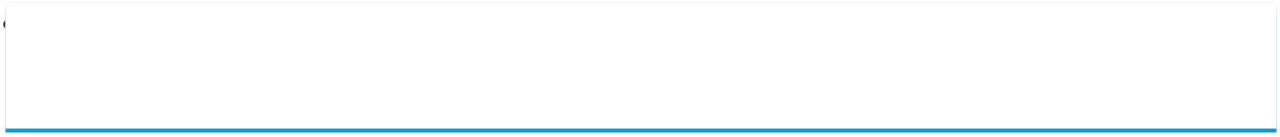
Toshiba TC90101FG Manual

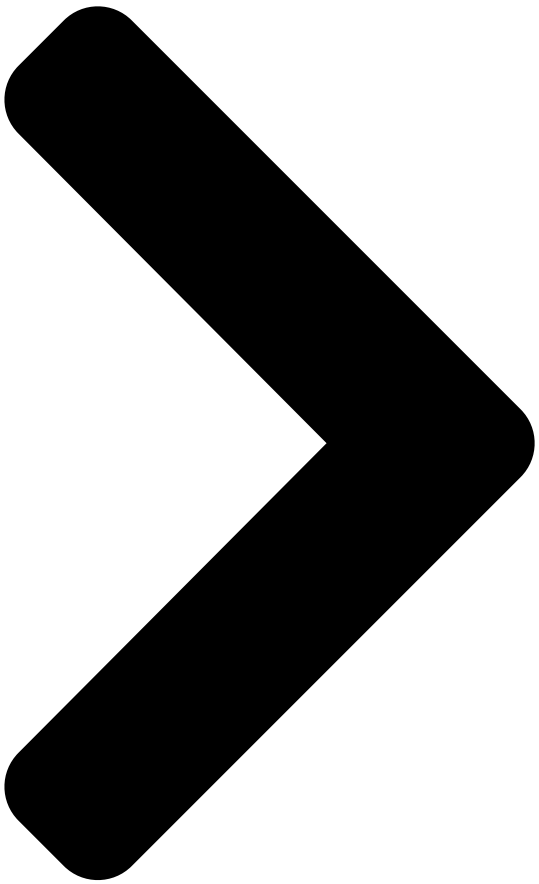
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35



-

Bookmarks



Y/C separation & Video Decoder

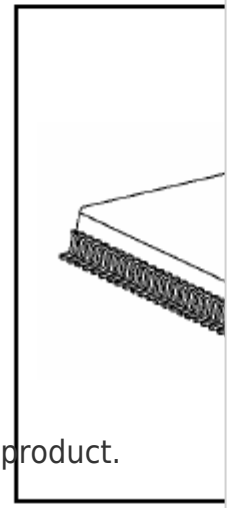
TC90101FG is a 1chip LSI of multi 3line comb and multi color decoder.
TC90101FG has built-in 2channels 8bit ADC and 2channels 8bit ADC for analog Video signal interface
and also include Y/C separation, color decode, and signal processing circuit.
The output interface of TC90101FG is a selectable for ITUR-601 & 656.

Featur

- Multi color system
  - Input I/F CVBS, Y/C, YcbCr(1H & 525p/625p)
  - Multi 3 line comb (SECAM: BPF)
  - Component signal frequency detection (525i/525p/625i/625p)
  - AGC circuit
  - Output format : 656/601
- Picture improvement

□□ Vertical enhance/LTI/Contrast/Setup adjust
C□ TOF/ACC/Color decode/color gain/CTI/offset adjust
• Noise level detection/ID1(525I & 525p) data slice/
CCD data slice/WSS data slice/ Macrovision detection

• I
2
C bus control
• Read data superposition on ITUR-656 output
• Package□ LQFP 100 □0.5mm pitch□
• Power supply□ 3.3 V□ 2.5V□1.5V



(note1)These devices are easy to be damaged by high voltage or electric fields.

In regards to this, please handle with care.

TOSHIBA is continually working to improve the quality and the reliability of its product.
●
Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
Feb./2005
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

□□□□□□□□□

TC90101FG

LQFP100-P-1414-0.5C
Weight□0.65g(Typ)
Version 4.2

Next Page

Related Manuals for Toshiba TC90101FG

Media Converter Toshiba TOSVERT VF-AS3 Instruction Manual

(32 pages)

Toshiba VEC008Z - Digital Encoder Manual

(article)

Media Converter Toshiba TOSVERT VF-nC3 Instruction Manual

(66 pages)

Media Converter Toshiba LF620 Instruction Manual

Electromagnetic flowmeter converter (160 pages)

Media Converter Toshiba TOSVERT VF-S15 Series Manual

(51 pages)

Media Converter Toshiba VEC008Z Installation Manual

Digital encoder (2 pages)

Media Converter Toshiba LF620 Manual

Electromagnetic flowmeter converter (8 pages)

Media Converter Toshiba TOSVERT VF-AS1 Instruction Manual

Expansion io card option 2 (19 pages)

Media Converter Toshiba TOSVERT VF-AS3 Instruction Manual

Rs485 communication function (20 pages)

Media Converter Toshiba USB001Z Instruction Manual

Usb-to-serial conversion unit (8 pages)

Media Converter Toshiba RS-485 Installation Manual

Usb to rs-485 converter port verification (8 pages)

Media Converter Toshiba USB001Z Instruction Manual

Toshiba usb-to-serial conversion unit instruction manual (17 pages)

Media Converter Toshiba RS4001Z-0 Instruction Manual

Rs485 converter unit (10 pages)

Media Converter Toshiba L5232 Instruction Manual

Electromagnetic flowmeter converter (174 pages)

Media Converter Toshiba RS4002Z-0 Instruction Manual

Rs485 converter unit (14 pages)

Summary of Contents for Toshiba TC90101FG

Page 1 TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications.

Page 2: Pin Layout

TC90101FG □□ B lock Diagram X'tal HD/VD Clock reference Sync Sep. × 8 Timing Clamp clock Gene. S/N detection macrovision CCD slice Vertical 10bit ADC CVBS enhance contrast adust ITU-R656 656/601 delay adjust encod□ 3line Format comb 8bit ADC □□□ color decord → 4fsc □□□□ adjust...

Page 3 TC90101FG □□Terminals discription Pi□ Pi□ Function Durable Circuit DC at Analog signal No Name □ □□Condition at normal operation □oltage (Analog or Digital)

normal Amplitude (V) Oparation (Vp-p) (V) 1 VREFDA
The reference voltage terminal of DAC 2.5 Bypass 1.5 - 2 VDDPLL
Power supply for X8 PLL circuit ...

Page 4 TC90101FG Pin Pin Function Durable Circuit DC at Analog signal (Analog or Digital) No Name () : Condition at normal operation voltage normal Amplitude (V) Oparation (Vp-p) (V) 51 TESTM6 Terminal for Test mode (Normaly connect to GND) 3.3 IN 0 - 52 COUT0 cbcr digital video signal output (LSB) 3.3 ...

Page 5: Functional Description

TC90101FG is a Video decoder device for multi color system (525i. 625i). TC90101FG also has a through mode and sync processing for 525p & 625p component signal. 1.TC90101FG has input interface for CVBS, S-Video, Ycbcr. For RGB signal it needs some external circuit as below.

Page 6 2.2 Input signal amplitude TC90101FG has a 10bit ADC for CVBS & Y signal and 2ch 8bit ADC for C & Cb/Cr. The Dynamic range of ADC is desgned as AVDD *0.4 (Normally 1Vpp at AVDD = 2.5V). The recomemdation amplitude of the input signal : 0.7Vpp at 140IRE (CVBS/Y) . refer to fig-1.

Page 7 The clam control circuit controls the corect clamping for input signals. TC90101FG has a feed back clamp for H-Sync portion of CVBS/Y input signal to clamp 256LSB(10bit unit). It is selectable to use the 2 types of the feed back clamp (internal circuit or external circuit) via IIC bus.

Page 8 6. D2 signal (525p/525p component) processing TC90101FG has D1 and D2 detection circuit and Sync processing for D2 signal. D2 signal is converted as 4:2:2 digital signal by internal ADC. (Sampling rate of Y ADC is 27MHz.) ID-1 data slice for 525p is available but It's not available to use picture implrovement function and Noise level detection, (The sliced data of ID-1 can be read via IIC.)

Page 9 TC90101FG e) CTI function f0 is selectable (1.7MHz/ 3.3MHz). Coring level is selectable (0.4IRE/ 0.8IRE/ 1.6IRE/ 3.2IRE). Gain is selectable (OFF/ x1/8 / x1/4 / x1/2). f) Offset control of the period of picture area The DC level of the Cb and Cr signals are controlled via IIC independently.

Page 10 TC90101FG (2 Field) 263 264 265 266 267 268 269 270 271 272 273 ... 282 CVBS ...

Page 11 TC90101FG (2 ,4 Field) CVBS 309 310 311 312 313 314 315 316 317 318 319 ... 335 336 HDOUT VDOUT 同期ｽﾙｰ Sync Through ﾓｰﾄﾞ Mode FIELD 2 ODD/EVEN VDOUT 656 準拠 Mode ﾓｰﾄﾞ ODD/EVEN FIELD 2 Selectable Sync through mode and 656 mode via THRHV at sub address 22hex. ...

Page 12 RUN-IN detection, start code detection and sliced data can be read via IIC bus. e) Macrovision detection TC90101FG can detect a pseudo sync, AGC pulse and color stripe. The result of Macrovision detection can be read via IIC bus.

Page 13 12. Insertion of IIC read data for output TC90101FG has IIC read data insert mode for ITU-656 out put format. It's also available for ITU-601 mode. These functions are based on ARIB STD-B6. Selection of the line for IIC read data insertion is set via register at sub address 25hex and 26hex .

Page 14 TC90101FG ●UWD <I2C Read Bus → 656 insertion specification.> In case of 1byte Read register (RD[7:0]), it is superposed as below ・Read register 1 byte. ・656 insertion: 1 word. D(-1) D(-2) (10bit mode) ・656 insertion: 2nd word...

Page 15: Data Transmission Format

TC90101FG 4. IIC BUS TC90101FG has two slave address (B2 hexand B0hex). A slave address is chosen by BUSSEL Terminal which is pin 24. (BUSSEL=L: B0hex , BUSSEL=H: B2hex)。
・Data transmission format ...

Page 16 TC90101FG IIC BUS MAP INSEL AUTODET TVM3 TVM2 TVM1 TVM0 Input signal selection FSC selection FV selection PAL selection SECAM selection

Color system detection mode 00□CVBS 00□Manual □00h-D5□□D2 : Active□ 0□3.58MHz 0□60Hz 0□Not PAL 0□Not SECAM 01□Y/C□S-Video□ 01□EU mode 1□4.43MHz □□50Hz 1□PAL 1□SECAM 10□YCbCr□D1or D2 Component□ 0000□NT358 0100□NT50 1000□NT443 1100□don't use 10□South America 11□CVBS+□CbCr(for SCART□ 11□Full detection mode 0001□don't use 0101□don't use 1001□SEC60 1101□SECAM...

Page 17 TC90101FG CICLMPPS CICLMPPW
Adjustment of input clamp phase for analog Cb/Cr
Adjustment of input clamp width for analog Cb/Cr 1000□-1.185μ□ □ 0000□± □ □ 0111□+1.04μ□ 1000□-1.185μ□ □ 0000□±□ □ 0111□+1.04μ□ INIT:00H
C ClampPulseF C ClampPulseW DIGITAL C CLAMP Adjustment of digital clamp phase for Cb/Cr Adjustment of digital clamp width for Cb/Cr Time constant of Cb/Cr digital clamp 000□1.19μ □ □ 111□3.26μ□ 000□0.9μ□ □ 111□2.96μ□ 00□OFF 10□mediam INIT:00H 01□small 11□large COLOR KILLER LEVEL ACC LEVEL CONFIX Adjustment the sensitivity of the killer detection Adjustment □□□ reference level Killer function 000□Max □ 111□□□□ 0000□□□□ □ 1111□□□ □ □Initial□1000□ 0□normal INIT:08H 1□killer off DOT DIST CGAIN COMB+ 1LINE DOT COM443N Reduse dot (Horizontal)

Page 18 TC90101FG BFPS VBIVAD[2:0] Adjustment start phase of burst gate
Adjustment the pase of VBI data slice 16LSB limit 0000□center □ 1111□+4.44μs 100:-4H□000:center □111:3H 0□OFF □0.296μs step□ INIT:00H 1□ON VPHS HDST BYFOFF BCFOFF Adjustment start phase of V at THRHV=1 Delay adjustment of HDOUT BSRY filter BSRC filter 110□384W 011□192W 000□0W 10□40w 00□32w 111□don't use 100□256W 001□64W 11□44w 01□36w 0□ON 0□ON INIT:03H (1W:27MHz) 101□320W 010□128W (1W:27MHz) 1□OFF...

Page 19 TC90101FG CCDDLY ID1DLY Phase adjustment for CCD data slice
Phase adjustment for ID1 data slice 0000:min □ 1000:center □ 1111:max 0000:min □ 1000:center □ 1111:max 1STEP = 128fh 1STEP = 128fh INIT:88H WSSDLY CDECEV1[4] YADFILON FILON□ FILON0 Phase adjustment for WSS data slice fsc pull in 13.5M trap IIR FILTER IIR FILTER 0000:min □ 1000:center □ 1111:max performance for ADC selection ON/OFF 1STEP = 128fh 0:Nornal 0□OFF 0:FIL1 0:OFF INIT:84H 1:Wide 1□ON 1:FIL2 1:ON PROG BUSFBCLMOD Time constant of theInternal...

Page 20 TC90101FG IIC BUS Read Data DET50 NOSIG NOVP FIELD UNLOCK H/VSTD progressive Field Frequency Signal det. V-Sync Sep Field indication HPLL for inpit sig H-V std. det. D1/D2 det. 0:60Hz 0:Signal det. 0:V sig det 0:ODD 0:LOCK 0:std. 0:D1 1:50Hz 1:no signal 1:no V sig 1:EVEN 1:UNLOCK 1:non-std. 1:D2 FSCSEL DET443 PALDET SECAMDET CKILL FSCLOCK 4.43MHz det.

Page 21 TC90101FG ●Additional information about IIC registers. BUS address Function Contents 00H□D7-D6 Input signal selection. An input signal is chosen. 00H□D5-D2 Select TVM. The TV-system is fixed forcibly. It uses when it is worked in the manual. 00H□D1-D0 Color system detection Setup Color system detection mode. mode.
Manual / Europeian / South American / Full auto detection. 01H□D7 Setup for YCS. 3-lineComb or BPF is chosen. 0: 3-line-Comb 1: B.P.F 01H□D5-D4 Select clock
Setup for an output clock frequency. Select “601□13.5MHz” or “656□27MHz”. 01H□D3 Select OUTPUT FORMAT Setup for an output format (601or656). 01H□D2 Select OUTBITS Setup for an output bits range (8bit or 10bit). 01H□D1 ...

Page 22 TC90101FG BUS address Function Contents 06H□D7-D0 Contrast Adjustment
It set the Contrast. (Reference value: [01000000]) Variability is ×0.5□×2.4.
□When use big value and inputs big amplitude signal,
It takes place over range of internal circuit.) 07H□D7-D0 Brightness Adjustment
It set the Brightness. Variability is -128LSB □ +128LSB. 08H□D7-D4 Cr Gain Adjustment
It set Gain of Cr. (Refrence value:[0000]) Variability is ×0.5□×1.4.
□When use big value and inputs big amplitude signal,
It takes place over range of internal circuit.) 08H□D3-D0 Cb Gain Adjustment
It set Gain of Cb. (Refrence value:[0000]) Variability is ×0.5□×1.4.
□When use big value and inputs big amplitude signal,
It takes place over range of internal circuit.) 09H□D7-D4 Cr Output OFFSET adjust.
Fine tune for offset of the Cr at output stage. 09H□D3-D0 Cb Output OFFSET adjust.
Fine tune for offset of the Cr at output stage. 0AH□D7-D1 HUE adjustment
HUE adjustment at the NTSC input mode. Variable is -45°-+43.6 °. 0AH□D0 ...

Page 23 TC90103FG SECAM Trap Frequency Response TC90101FG
SECAM Trap Frequency Response - 10BUS ...

Page 24 TC90101FG BUS address Function Contents 14H□D7-D6 Selection for
It select the input signal of Composite-SYNC-in of Pin-33. external-sync
[00]: OFF(Internal) Pin33 must be connect to GND.
[01]: External composite Sync mode (polarity: High)
[10]: External composite Sync mode (polarity: Low) [11]: External V-Sync mode (polarity: High)
14H□D5 Sync Separation level Level of Sync-sepa is set up. Initial value is [0]:30%. 14H□D4-
D3 Sync-tip-clamp-mode for It set the control of clamp. CVBS
[00]: Sync tip clamp ON [01]: Sync tip clamp OFF [10]: AUTO1(Sync-tip-
clamping becomes activity, When it detect non-signal or pedestal has a big difference.
[11]: AUTO2 (Sync-tip-clamping becomes activity, When it detect non-signal. 14H□D2
Setup for V-sepa Setup for V-sepa 0: Type 1
1: Type 2 (Type 2 is more effective than Type1.) 14H□D1 V-sepa limit Limit of V-
sepa is set up. V-sepa becomes easy, when it is set up in 1/16. But,Usually use with 0(1/8□.
14H□D0 Setup of Half-H-killer It count Half-H at the V period. ...

Page 25 TC90101FG BUS address Function Contents 19H□D7-D4 Threshold level at the
Threshold level that Phase-diffrent changes from Big to middle phase difference big is set up.
to middle Recommendation value: [0100] 19H□D3-D0 Threshold level at the
Threshold level that Phase-diffrent changes from middle to phase difference middle
Big is set up. to big Recommendation value: [01000] 1AH□D7-D5 Start phase for noise The
horizontal-start-phase of the detection of Noise is set up.
“Point of 5.3µs from sync” is center. detection 1AH□D4-D2 Width for noise The horizontal-
width of the detection of Noise is set up. detection The amount of noise-
detection changes by Width. ...

Page 26 TC90101FG BUS address Function Contents 20H□D3-D1 Set line of VBI data
The line of VBI-data-slice is set up. slice Usually used with center.
When it uses at the outside synchronism, it uses for the adjustment, when the phase of the
outside VD-pulse and the input
signal are shifted. VBI and Macrovision detection line move at the same time, too. 20H□D0
16LSB limit It limit less than 16LSB at the Digital output.
Use by ON, when you use with 601/656 output. 21H□D7-D5 Start phase of V at
The phase of VD is set up. THR-V Bus:111 can't be set up. 21H□D4-D3 Delay adjustment of
When Thru of V, Set the delay of HD-Pulse.The variability is HD-OUT
32W□44W (1W=27MHz). ...

Page 27 TC90101FG BUS address Function Contents 24H□D2 AFC leak control
It is Leak-control in the AFC circuit. It usually uses on OFF. 24H□D1-D0 The order of read Data
It can change order that Read-data. 00: ABCD A□Detection□B□CCD□C□ID1□D□WSS
BUS□01=BCAD□BUS□10=CABD□BUS□11=DABC 25H□D7 Data insert of H It insert Read-
data to the H period of the output. Data is inserted after EAV at 656.
Data is inserted same place with 656 at 601. 25H□D6 Data insert of V It insert Read-
data to the V period of the output. Data is inserted after EAV at 656.
Data is inserted same place with 656 at 601. 25H□D5 Data insert for 601
Data can insert on either of Y or CbCr at 601 output. Data cannot insert both line. 25H□D4-D0
Line number for insert Set line which Read-Data insert. Data. It can set each 1-line for 1bit.
26H□D7-D4 Line number for insert ...

Page 28 TC90101FG BUS address Function Contents 2BH□D1-D0
An integral coefficient It is the integral-coefficient of Peak AGC detection.
of Peak AGC detection 2CH□D7 Sync AGC It set ON/OFF of Sync AGC. 2CH□D3-D2
Sync AGC attack time It set Sync AGC attack time. 2CH□D1-D0 Peak/Sync AGC recovery
It set recovery time of Peak AGC and Sync AGC. time 2DH□D7 LPF for CCD
It set ON/OFF of LPF for CCD. 2DH□D6 CCD slice function mode
It set mode of CCD slice function. Level changes by the input amplitude,when Auto mode. 2DH□
D5 CCD slice level It set CCD slice level. It is effective when 2DH:D6 is set a fix. 2DH□D3
Phase width of ID1 It set phase width of ID1 detection. detection 2DH□D2
CCD Start bit detection It is the detection sensitivity of the start bit of CCD. ...

Page 29 TC90101FG BUS address Function Contents 32H□D7 D1/D2 Det
It is the distinction of D1/D2. It is effective 32H:D6 when manual set. 32H□D6
D1/D2 Manual set Internal control is fixed with D1orD2. 32H□D5-D4 Internal feed-back-
When clamp set internal, it can set time constant. clamp 33H□D7 Manual Gain AGC
It set ON/OFF of Peak-AGC Gain. It is effective when it is ON.
It gives priority to Manual when this bit is ON. Therefore, it can't get the effect of AGC. 33H□D6-
D0 Manual Gain It is effective when 33H(D7). Gain becomes a fix. 34H□D7-D4
CGP start phase It set start phase of CGP(Output of Terminal-73). 34H□D3-D0 Width of CGP
It set width of CGP(Output of Terminal-73). 35H□D7-D4 Threshold for DET.443

It set threshold for DET.443. It is easy to distinguish when a MAX side is chosen. 35H□D1-D0 Sync-tip-clamp-mode for ...

Page 30 TC90101FG MAXIMUN RATINGS□Vss=0V, Ta=25℃□ Each item of the maximum rating shows the marginal value of this product. Since a product is sometimes damaged when rating is exceeded also one item or for a moment again, be sure to use it within rating. ...

Page 31 TC90101FG The condition of power (VDD=3.3V, 2.5V, 1.5V) rising and falling (1)Power Supply rising These contents are the important items which influence the reliability guarantee of the IC. It is necessary to satisfy the following condition. ...

Page 32 TC90101FG ELECTRICAL CHARACTERRISTICS (1) DC CHARACTERRISTICS □Ta=25℃,VDD1=1.50±0.1V,VDD2=2.50±0.2V,VDD3=3.30±0.3V) ITEM Terminal No. Symbol Min. Typ. Max. Unit Note Power 15,32,39,54,66 IDD1 30 45 70 mA Sum total current of 1.5V Supply system power supply terminal Current NTSC:Y/C IN, Color Bar Signal 2,82,89,95,97 IDD2 80 105 135 ...

Page 33 TC90101FG (2) AC CHARACTERRISTICS □Ta=25℃,VDD1=1.50V,VDD2=2.50V,VDD3=3.30V) ITEM Symbol Min. Typ. Max. Unit Note AD input level for Y VYIN 0.7 0.8 Vp-p White 100% Signal AD input level for C VCIN 0.5 0.8 Vp-p Cb/Cr input ADC differentiation error DLEa ±4 LSB ADC integration error ILEa ...

Page 34 TC90101FG Application ② 1.5V 3.3V 1.5V 5 6 5 5 5 2 5 1 BIASYAD TESTM5 0.01µ ② 3.3V VRTYAD VDDIO1 0.01µ 0.01µ CKOUT NP 0.47µ VSSYAD YOUT0 ① VRMYAD YOUT1 0.01µ CVBS IN TC90101FG VSSIO1 0.1µ...

Page 35 TC90101FG ● PACKAGE OUTLINE LQFP100-P-1414-0.50C UNIT:mm ...