



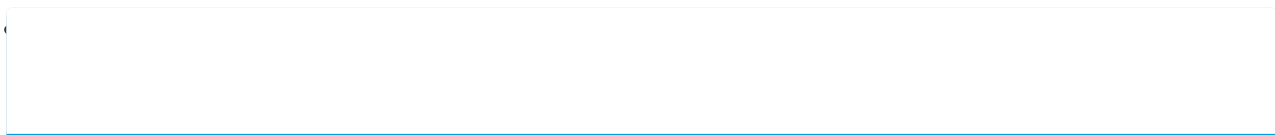
Asus AAEON COM-TGUC6 User Manual

Com express module

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Smart display module (82 pages)

[Control Unit Asus Aaeon NIM-S26B Quick Installation Manual](#)

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Summary of Contents for Asus AAEON COM-TGUC6

[Page 1](#) COM-TGUC6 COM Express Module User's Manual 2 Last Updated: January 26, 2024...

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[Page 3](#) Acknowledgements All other products' name or trademarks are properties of their

respective owners. Microsoft Windows is a registered trademark of Microsoft Corp. • Intel®, Iris® and Celeron® are registered trademarks of Intel Corporation • Intel Core™ is a trademark of Intel Corporation •...

[Page 4](#) Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity COM-TGUC6 • If any of these items are missing or damaged, please contact your distributor or sales representative immediately. Preface...

[Page 5](#) About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the product page at AAEON.com for the latest version of this document.

[Page 6](#) Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

[Page 7](#) If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

[Page 8](#) FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

[Page 9](#) China RoHS Requirements (CN) AAEON Main Board/ Daughter Board/ Backplane (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) SJ/T 11363-2006 X...

[Page 10](#) China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Main Board/ Daughter Board/ Backplane Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) PCB &...

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Chapter 1 Chapter 1 - Product Specifications..

[Page 14: Specifications](#)

Specifications System Form Factor COM Express Compact Size, Type 6 11th Generation Intel® Core™ Processors: Intel® Core™ i7-1185G7E (4C/8T, 1.8 GHz, 15W) Intel® Core™ i5-1145G7E (4C/8T, 1.5 GHz, 15W) Intel® Core™ i3-1115G4E (2C/4T, 2.20 GHz, 15W) Intel® Celeron® Processor 6000 Series: Intel®...

[Page 15](#) Display Graphics Controller Intel® Iris® Xe Graphics Intel® UHD Graphics Video Output 4 Simultaneous Displays: DDI x 3, up to 3840 x 2160 18/24-bit Single/Dual-Channel

LVDS/eDP x 1, up to 1920 x 1080/3840 x 2160 VGA x 1, up to 1920 x 1080 Ethernet Intel®...

[Page 16](#) Environmental Operating Temperature 32°F ~ 140°F (0°C ~ 60°C) Storage Temperature -40°F ~ 185°F (-40°C ~ 85°C) Operating Humidity 0% ~ 90% relative humidity, non-condensing CE/FCC Class A Weight 0.44 lb. (0.20Kg) Chapter 1 - Product Specifications...

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Block Diagram Chapter 1 - Product Specifications...

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Chapter 2 Chapter 2 - Hardware Information...

[Page 19: Dimensions](#)

Dimensions Chapter 2 - Hardware Information...

[Page 20](#) With Active Cooling (Part No: COM-TGUC6-FAN01) With Heat Spreader (Part No: COM-TGUC6-HSP01) Chapter 2 - Hardware Information...

[Page 21: Jumpers And Connectors](#)

Jumpers and Connectors Component Side Chapter 2 - Hardware Information...

[Page 22](#) Solder Side Chapter 2 - Hardware Information...

[Page 23: List Of Connectors](#)

List of Connectors Please refer to the table below for all of the board's connectors that you can configure for your application Label Function COMAB1 Express Row A/B Connector COMCD1 Express Row C/D Connector DDR1 DDR4 SODIMM COM Connector DDR2 DDR4 SODIMM COM Connector 2.3.1 COM Express Row A/B Connector (CN2)

[Page 24](#) Row A Row B Signal Signal SATA0_TX+ SATA1_TX+ SATA0_TX- SATA1_TX- SUS_S4# SUS_STAT# SATA0_RX+ SATA1_RX+ SATA0_RX- SATA1_RX- GND (FIXED) GND (FIXED) SUS_S5# PWR_OK BATLOW# (S)ATA_ACT# AC/HDA_SYNC HDA_SDIN1 AC/HDA_RST# HDA_SDIN0 GND (FIXED) GND (FIXED) HDA_BITCLK SPKR HDA_SDOOUT I2C_CK BIOS_DIS0# I2C_DAT THRMTRIP# THRM# USB6- USB7- USB6+...

[Page 25](#) Row A Row B Signal Signal USB2+ USB3+ USB_2_3_OC# USB_0_1_OC# USB0- USB1- USB0+ USB1+ VCC_RTC RSMRST#_A48 SYS_RESET# LPC_SERIRQ CB_RESET# GND (FIXED) GND (FIXED) GPIO GPO1 PCIE_TX4+ PCIE_RX4+ PCIE_TX4- PCIE_RX4- GPO2 PCIE_TX3+ PCIE_RX3+ PCIE_TX3- PCIE_RX3- GND (FIXED) GND (FIXED) PCIE_TX2+ PCIE_RX2+ PCIE_TX2- PCIE_RX2- GPI1...

[Page 26](#) Row A Row B Signal Signal GND (FIXED) GND (FIXED) LVDS_A0+ LVDS_B0+ LVDS_A0- LVDS_B0- LVDS_A1+ LVDS_B1+ LVDS_A1- LVDS_B1- LVDS_A2+ LVDS_B2+ LVDS_A2- LVDS_B2- LVDS_VDD_EN LVDS_B3+ LVDS_A3+ LVDS_B3- LVDS_A3- LVDS_BKLT_EN GND (FIXED) GND (FIXED) LVDS_A_CK+ LVDS_B_CK+ LVDS_A_CK- LVDS_B_CK- LVDS_I2C_CK LVDS_BKLT_CTRL LVDS_I2C_DAT VCC_5V_SBY GPI3 VCC_5V_SBY KB_RST#(Option)

[Page 27](#) Row A Row B Signal Signal SPI_CS# SER0_TX SMI#(Option) SER0_RX SCI#(Option) A100 GND (FIXED) B100 GND (FIXED) A101 SER1_TX B101 FAN_PWMOUT A102 SER1_RX B102 FAN_TACHIN A103 LID# B103 SLEEP# A104 VCC_12V B104 VCC_12V A105 VCC_12V B105 VCC_12V A106 VCC_12V B106 VCC_12V A107 VCC_12V...

[Page 28: Com Express Row C/D Connector \(Cn3\)](#)

2.4.2 COM Express Row C/D Connector (CN3) Row C Row D Signal Signal GND (FIXED) GND (FIXED) USB_SSRX0- USB_SSTX0- USB_SSRX0+ USB_SSTX0+ USB_SSRX1- USB_SSTX1- USB_SSRX1+ USB_SSTX1+ USB_SSRX2- USB_SSTX2- USB_SSRX2+ USB_SSTX2+ GND (FIXED) GND (FIXED) USB_SSRX3- USB_SSTX3- USB_SSRX3+ USB_SSTX3+ DDI1_CTRLCLK_AUX+ DDI1_CTRLCLK_AUX- GND_C18 GND (FIXED) GND (FIXED) DDI1_HPD...

[Page 29](#) Row C Row D Signal Signal DDI1_PAIR0+ DDI1_PAIR0- DDI1_PAIR1+ DDI1_PAIR1- GND (FIXED) DDI2_CTRLCLK_AUX+ DDI1_PAIR2+ DDI2_CTRLCLK_AUX- DDI1_PAIR2-

DDI2_DDC_AUX_SEL DDI1_DDC_AUX_SEL DDI3_CTRLCLK_AUX+ DDI1_PAIR3+
DDI3_CTRLDATA_AUX- DDI1_PAIR3- DDI3_DDC_AUX_SEL GND_D38 DDI3_PAIR0+ DDI2_PAIR0+
DDI3_PAIR0- DDI2_PAIR0- GND(FIXED) GND (FIXED) DDI3_PAIR1+ DDI2_PAIR1+ DDI3_PAIR1-
DDI2_PAIR1- DDI3_HPD DDI2_HPD GND_D45 DDI3_PAIR2+ DDI2_PAIR2+ DDI3_PAIR2-
DDI2_PAIR2- GND_D48...

[Page 30](#) Row C Row D Signal Signal PEG_RX0- PEG_TX0- PEG_LANE_RV# PEG_RX1+
PEG_TX1+ PEG_RX1- PEG_TX1- TYPE2# PEG_RX2+ PEG_TX2+ PEG_RX2- PEG_TX2- GND(FIXED)
GND(FIXED) PEG_RX3+ PEG_TX3+ PEG_RX3- PEG_TX3- GND_C63 GND_D63 GND_C64 GND_D64
GND (FIXED) GND (FIXED) GND_C77 GND_D77 Chapter 2 - Hardware Information...

[Page 31](#) Row C Row D Signal Signal GND (FIXED) GND (FIXED) GND_C83 GND_D83 GND
(FIXED) GND (FIXED) GND_C97 GND_D97 C100 GND (FIXED) D100 GND (FIXED) C101 D101
C102 D102 C103 D103 C104 VCC_12V D104 VCC_12V C105 VCC_12V D105 VCC_12V C106
VCC_12V D106 VCC_12V Chapter 2 -...

[Page 32](#) Row C Row D Signal Signal C107 VCC_12V D107 VCC_12V C108 VCC_12V D108
VCC_12V C109 VCC_12V D109 VCC_12V C110 GND (FIXED) D110 GND (FIXED) Chapter 2 -
Hardware Information...

[Page 33: Chapter 3 - Ami Bios Setup](#)

Chapter 3 Chapter 3 - AMI BIOS Setup...

[Page 34: System Test And Initialization](#)

System Test and Initialization The board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

[Page 35: Ami Bios Setup](#)

AMI BIOS Setup The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off. To enter Setup, power on the computer and press ...

[Page 36: Setup Submenu: Main](#)

Setup Submenu: Main Chapter 3 - AMI BIOS Setup...

[Page 37: Setup Submenu: Advanced](#)

Setup Submenu: Advanced Chapter 3 - AMI BIOS Setup...

[Page 38: Graphics Configuration](#)

3.4.1 Graphics Configuration Options Summary VBT Select LVDS On eDP On eDP/LVDS Off
Optimal Default, Failsafe Default Select VBT for GOP Driver. Chapter 3 - AMI BIOS Setup...

[Page 39: Lvds Panel Configuration](#)

3.4.1.1 LVDS Panel Configuration Options Summary Panel Type 640x480@60Hz 800x480@60Hz
800x600@60Hz 1024x600@60Hz 1024x768@60Hz Optimal Default, Failsafe Default
1280x768@60Hz 1280x800@60Hz 1280x1024@60Hz 1366x768@60Hz 1440x900@60Hz
1600x1200@60Hz 1920x1080@60Hz 1920x1200@60Hz Select panel type. Chapter 3 - AMI
BIOS Setup...

[Page 40](#) Options Summary Color Depth 18-Bit Optimal Default, Failsafe Default 24-Bit 36-Bit
48-Bit Select panel type. Backlight Mode BIOS & Application Windows Slider Optimal Default,
Failsafe Default Select backlight control signal type. Chapter 3 - AMI BIOS Setup...

[Page 41: Cpu Configuration](#)

3.4.2 CPU Configuration Options Summary Active Processor Cores Optimal Default, Failsafe
Default Number of cores to enable in each processor package. Turbo Mode Disabled Enabled
Optimal Default, Failsafe Default Enable/Disable processor Turbo Mode (requires EMTTM

enabled too). AUTO means enabled. Hyper-Threading Disabled Enabled...

[Page 42](#) Options Summary Intel (VMX) Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. Chapter 3 - AMI BIOS Setup...

[Page 43: Memory Configuration](#)

3.4.3 Memory Configuration Options Summary In-Band ECC Support Disabled Enabled Optimal Default, Failsafe Default Enable/Disable In-Band ECC. Either the IBECC or the TME can be enabled. In-Band ECC Error Injection Disabled Optimal Default, Failsafe Default Enabled By enabling this Error Injection feature, the user acknowledges the security risks. Enabling Error Injection allows attackers who have access to the Host Operating System to inject IBECC errors that can cause unintended memory corruption and enable the leak of security data in the BIOS stolen memory regions.

[Page 44: On-Module H/W Monitor](#)

3.4.4 On-Module H/W Monitor Chapter 3 - AMI BIOS Setup...

[Page 45: Smart Fan Mode Configuration](#)

3.4.4.1 Smart Fan Mode Configuration FAN 1: Full Mode Options Summary FAN 1 Full Mode Optimal Default, Failsafe Default Manual Mode by PWM Auto Mode by PWM Smart Fan Mode Select. PWM signal Non-inverting Optimal Default, Failsafe Default Inverting Select output PWM of inverting or non-inverting signal. Chapter 3 -...

[Page 46](#) FAN 1: Manual Mode by PWM Options Summary Manual Setting Optimal Default, Failsafe Default Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number: Chapter 3 - AMI BIOS Setup...

[Page 47](#) FAN 1: Auto Mode by PWM Options Summary Monitor Thermal CPU Temperature (PECI) Optimal Default, Failsafe Default Thermal Source 1(T1) Thermal Source 2(T2) Select monitor thermal source. Temperature of Start Optimal Default, Failsafe Default Temperature of Start. Temperature of Off Optimal Default, Failsafe Default Temperature of Off.

[Page 48: Pch-Fw Configuration](#)

Options Summary 64 (PWM) Slope (PWM) 3.4.5 PCH-FW Configuration Chapter 3 - AMI BIOS Setup...

[Page 49: Firmware Update Configuration](#)

3.4.6.1 Firmware Update Configuration Options Summary Me FW Image Re-Flash Disabled Optimal Default, Failsafe Default Enabled Enable/ Disable Me FW Image Re-Flash Function. FW Update Disabled Enabled Optimal Default, Failsafe Default Enable/Disable ME FW Update Function Chapter 3 - AMI BIOS Setup...

[Page 50: On-Module Configuration](#)

3.4.6 On-Module Configuration Options Summary Battery Management Disabled Optimal Default, Failsafe Default One Battery Enable to support battery in ACPI OS by I2C_CK, I2C_DAT (B33, B34). EC-SMB-HC Support Disabled Optimal Default, Failsafe Default Enabled SMBus Host Controller Interface via Embedded Controller. Chapter 3 -...

[Page 51: Power Management](#)

3.4.7 Power Management Options Summary Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select system power mode. Restore AC Power Loss Last State Always On Always Off Optimal Default, Failsafe Default SIO Restore AC Power Loss: To decide the behavior after system power cut then resupply.

[Page 52: Aaeon Bios Robot](#)

3.4.8 AAEON BIOS Robot Options Summary Sends watch dog before Disabled Optimal Default, Failsafe Default BIOS POST Enabled Enabled - Robot set Watch Dog Timer (WDT) right after power on, before BIOS start POST process. And then Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to

zero.

[Page 53](#) Options Summary Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this before 'Send watch dog'. Delayed POST Disabled Optimal Default, Failsafe Default (DXE phase)

[Page 54: Setup Submenu: System I/O](#)

Setup Submenu: System I/O Chapter 3 – AMI BIOS Setup...

[Page 55: Pci Express Configuration](#)

3.5.1 PCI Express Configuration Options Summary PCI Express Root Port 1 Disabled Enabled Optimal Default, Failsafe Default Control the PCI Express Root Port. PCIe Speed Auto Optimal Default, Failsafe Default Gen1 Gen2 Gen3 Gen4 Configure PCIe Speed. Chapter 3 – AMI BIOS Setup...

[Page 56](#) Options Summary Hot Plug Disabled Optimal Default, Failsafe Default Enabled PCI Express Hot Plug Enable/Disable. PCIe 0_3 Select PCIe Controller are four Optimal Default, Failsafe Default ×1 PCIe Controller are one ×2 and two ×1 PCIe Controller are two ×2 PCIe Controller is one ×4 PCIe Controller Selection.

[Page 57](#) Options Summary PCIe Speed Gen2 Gen3 Configure PCIe Speed. Hot Plug Disabled Optimal Default, Failsafe Default Enabled PCI Express Hot Plug Enable/Disable. PCI Express 3 Disable Enable Optimal Default, Failsafe Default Control the PCI Express Root Port. PCIe Speed Auto Optimal Default, Failsafe Default Gen1 Gen2...

[Page 58: Storage Configuration](#)

3.5.2 Storage Configuration Options Summary SATA Controller(s) Enabled Optimal Default, Failsafe Default Disabled Enable/Disable SATA Device. Port 0 Disabled Enabled Optimal Default, Failsafe Default Enable or Disable SATA Port. Hot Plug Disabled Optimal Default, Failsafe Default Enabled Designates this port as Hot Pluggable. SATA Device Type Hard Disk Drive Optimal Default, Failsafe Default...

[Page 59](#) Options Summary Hot Plug Disabled Optimal Default, Failsafe Default Enabled Designates this port as Hot Pluggable. SATA Device Type Hard Disk Drive Optimal Default, Failsafe Default Solid State Drive Identify the SATA port is connected to Solid State Drive or Hard Disk Drive. Chapter 3 –...

[Page 60: Hd Audio Configuration](#)

3.5.3 HD Audio Configuration Options Summary HD Audio Disabled Enabled Optimal Default, Failsafe Default Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled. Chapter 3 – AMI BIOS Setup...

[Page 61: Digital Io Port Configuration](#)

3.5.4 Digital IO Port Configuration Options Summary GPI* Input Optimal Default, Failsafe Default Output Set DIO as Input or Output. GPO* Input Output Optimal Default, Failsafe Default Set DIO as Input or Output. Output Level High Optimal Default, Failsafe Default Set output level when DIO pin is output.

[Page 62: Legacy Logical Devices Configuration](#)

3.5.5 Legacy Logical Devices Configuration Chapter 3 – AMI BIOS Setup...

[Page 63: Serial Port 1 Configuration](#)

3.5.5.1 Serial Port 1 Configuration Options Summary Use This Device Disabled Enabled Optimal Default, Failsafe Default Enable or Disable this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=3F8h; IRQ=4; DMA; IO=2C8h; IRQ=11; DMA; Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

[Page 64: Serial Port 2 Configuration](#)

3.5.5.2 Serial Port 2 Configuration Options Summary Use This Device Disabled Enabled Optimal Default, Failsafe Default Enable or Disable this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2F8h; IRQ=3 DMA; IO=2D8h; IRQ=10; DMA; Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

[Page 65: Serial Port Console Redirection](#)

3.5.6 Serial Port Console Redirection Options Summary Console Redirection EMS Disabled Optimal Default, Failsafe Default Enabled Console Redirection Enable or Disable. Chapter 3 - AMI BIOS Setup...

[Page 66: Setup Submenu: Security](#)

Setup Submenu: Security Change Administrator/User Password You can set an Administrator password. If you set an Administrator password, you can then set a User password. User passwords do not have access to many of the features in the Setup utility. Select the password you want to set and press <Enter>.

[Page 67: Trusted Computing](#)

3.6.1 Trusted Computing Options Summary Security Device Support Disable Optimal Default, Failsafe Default Enable Enables or Disables BIOS support for security device. O.S. will not show Security Device. TGU EFI protocol and INT1A interface will not be available. SHA-1 PCR Bank Disabled Optimal Default, Failsafe Default Enabled...

[Page 68](#) Options Summary Pending operation None Optimal Default, Failsafe Default TPM Clear Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device. Platform Hierarchy Disabled Enabled Optimal Default, Failsafe Default Enable or Disable Platform Hierarchy.

[Page 69: Secure Boot](#)

3.6.2 Secure Boot Options Summary Secure Boot Disabled Optimal Default, Failsafe Default Enabled Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset. Secure Boot Mode Standard Custom...

[Page 70: Key Management](#)

3.6.2.1 Key Management Options Summary Factory Key Provision Disabled Optimal Default, Failsafe Default Enabled Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode. Chapter 3 - AMI BIOS Setup...

[Page 71: Setup Submenu: Boot](#)

Setup Submenu: Boot Options Summary Quiet Boot Disabled Enabled Optimal Default, Failsafe Default Enables or Disables Quiet Boot option. Network Stack Disabled Optimal Default, Failsafe Default UEFI Enable/Disable UEFI Network Stack. Chapter 3 - AMI BIOS Setup...

[Page 72: Setup Submenu: Save & Exit](#)

Setup Submenu: Save & Exit Chapter 3 - AMI BIOS Setup...

[Page 73: Chapter 4 - Drivers Installation](#)

Chapter 4 Chapter 4 - Drivers Installation...

[Page 74: Drivers Download And Installation](#)

Drivers Download and Installation Drivers for the COM-TGUC6 can be downloaded from the product page on the AAEON website by following this link: <https://www.aaeon.com/en/p/com-express-cpu-modules-com-tguc6> Download the driver(s) you need and follow the steps below to install them. Audio Driver (Windows 10) Open the folder where you unzipped the Audio Drivers Run the Setup.exe in the folder Follow the instructions...

[Page 75](#) LAN Drivers (Windows 10) Open the folder where you unzipped the LAN Drivers Read the ReadMe.txt file before proceeding. Caution: Be sure to install the driver package before

installing the Intel® PROSet package. Open the Wired_driver_26.3_x64 folder Run the Wired_driver_26.3_x64.exe file in the folder Follow the instructions, drivers will be installed automatically.

[Page 76: Appendix A - Watchdog Timer](#)

Appendix A Appendix A - Watchdog Timer...

[Page 77: Watchdog Timer Initial Program](#)

Watchdog Timer Initial Program Table 1: Embedded BRAM Relative Register Table Default Value Note Index 0x284(Note1) BRAM Index Register Data 0x285(Note2) BRAM Data Register Logical Device Number 0xA8(Note3) Watch dog Logical Device Number Function and Device Number 0x00(Note4) Watch dog Function/Device Number Table 2: Watchdog Relative Register Table Option BitNum...

[Page 78](#) *****
// Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex
//This parameter is represented from Note1 #define byte EcBRAMData //This parameter is represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3 #define byte BRAMFnDataReg //This parameter is represented from Note4 #define void EcBRAMWriteByte(byte Offset, byte Value);...

[Page 79](#) *****
Main VOID // Procedure : AaeonWDTConfig // (byte)Timer : Time of WDT timer.(0x00~0xFF) // (boolean)Unit : Select time unit(0: second, 1: minute). AaeonWDTConfig(); // Procedure : AaeonWDTEnable // This procedure will enable the WDT counting. AaeonWDTEnable();
***** Appendix A
- Watchdog Timer Programming...

[Page 80](#) *****
// Procedure : AaeonWDTEnable AaeonWDTEnable () VOID WDTEnableDisable(// Procedure : AaeonWDTConfig AaeonWDTConfig () VOID // Disable WDT counting WDTEnableDisable(// WDT relative parameter setting WDTParameterSetting(); WDTEnableDisable(byte Value) VOID ECBRAMWriteByte(TimerReg , Value); WDTParameterSetting() VOID Byte TempByte; // Watchdog Timer counter setting ECBRAMWriteByte(TimerReg , TimerVal);...

[Page 81](#) *****
ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value) VOID IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg); IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData, 0x30); //Write start ECBRAMReadByte(byte OPReg) Byte IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData, 0x10);...

[Page 82: Appendix B - I/O Information](#)

Appendix B Appendix B - I/O Information...

[Page 83: I/O Address Map](#)

I/O Address Map Appendix B - I/O Information...

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IRQ Mapping Chart Appendix B - I/O Information...

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Appendix C Appendix C - Programming Digital I/O...

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Digital I/O Programming The COM-TGUC6 utilizes an AAEON chipset as its Digital I/O controller. Below are the procedures to complete its configuration, which you can use to develop a customized program to fit your application. C.2 Digital I/O Register Table 1: Embedded BRAM Relative Register Table Default Value Note Index...

[Page 100: C.3 Digital I/O Sample Program](#)

C.3 Digital I/O Sample Program

```
***** //  
Embedded BRAM relative definition (Please reference to Table 1) #define byte EcBRAMIndex  
//This parameter is represented from Note1 #define byte EcBRAMData //This parameter is  
represented from Note2 #define byte BRAMLDNReg //This parameter is represented from Note3  
#define byte BRAMFnData0Reg //This parameter is represented from Note4...
```

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```
***** Main VOID  
Boolean PinStatus ; // Procedure : AaeonReadPinStatus // Input : Example, Read Digital I/O Pin 3  
status // Output : InputStatus : 0: Digital I/O Pin level is low 1: Digital I/O Pin level is High  
PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit); // Procedure :  
AaeonSetOutputLevel // Input : Example, Set Digital I/O Pin 6 level...
```

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```
*****  
AaeonReadPinStatus(byte OptionReg, byte BitNum) Boolean Byte TempByte; TempByte =  
ECBRAMReadByte(BRAMFnData1Reg, OptionReg); If (TempByte & BitNum == 0) Return 0;  
Return 1; AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value) VOID Byte  
TempByte; TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg); TempByte |= (Value  
<< BitNum); ECBRAMWriteByte(OptionReg, BitNum, Value);...
```

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```
*****  
ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value) VOID IOWriteByte(EcBRAMIndex, 0x10);  
IOWriteByte(EcBRAMData, BRAMLDNReg); IOWriteByte(EcBRAMIndex, 0x11);  
IOWriteByte(EcBRAMData, BRAMFnDataReg); IOWriteByte(EcBRAMIndex, 0x13 + OPReg);  
IOWriteByte(EcBRAMData, Value); IOWriteByte(EcBRAMIndex, 0x12); IOWriteByte(EcBRAMData,  
0x30); //Write start ECBRAMReadByte(byte FnDataReg, byte OPReg) Byte
```

```
IOWriteByte(EcBRAMIndex, 0x10); IOWriteByte(EcBRAMData, BRAMLDRReg);  
IOWriteByte(EcBRAMIndex, 0x11); IOWriteByte(EcBRAMData, FnDataReg);  
IOWriteByte(EcBRAMIndex, 0x12);...
```