Asus AAEON PICO-ADN4 User Manual

Pico-itx single board computer

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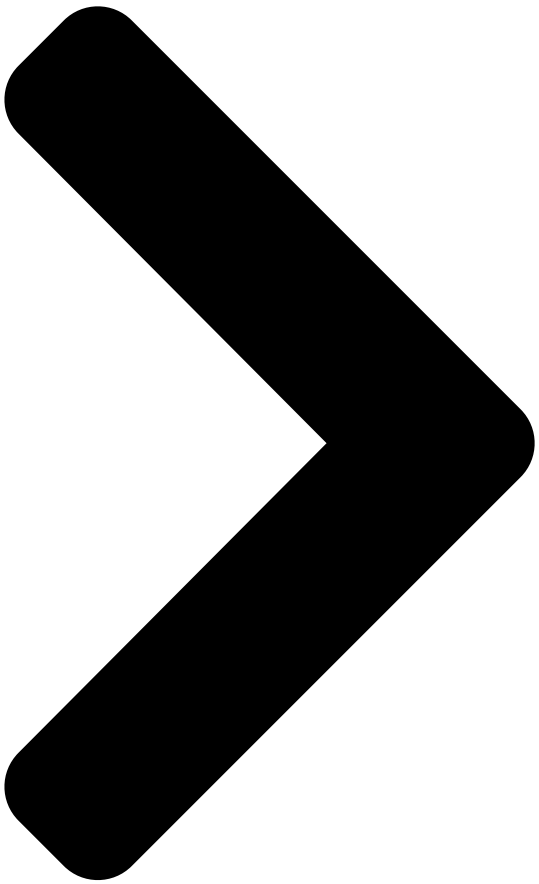

PICO-ADN4

PICO-ITX Single Board Computer

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User's Manual 1
Ed

Last Updated: November 8, 2023

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(14 pages)

Summary of Contents for Asus AAEON PICO-ADN4

Page 1 PICO-ADN4 PICO-ITX Single Board Computer User’s Manual 1 Last Updated: November 8, 2023...

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respective owners. Microsoft Windows® is a registered trademark of Microsoft Corp. • Intel® and Atom® are registered trademarks of Intel Corporation • ITE is a trademark of Integrated Technology Express, Inc. •...

Page 4 Packing List Before setting up your product, please make sure the following items have been shipped: Item Quantity PICO-ADN4 • If any of these items are missing or damaged, please contact your distributor or sales representative immediately. Preface...

Page 5 About this Document This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product. Users may refer to the product page on AAEON.com for the latest version of this document.

Page 6 Safety Precautions Please read the following safety instructions carefully. It is advised that you keep this manual for future references All cautions and warnings on the device should be noted. Make sure the power source matches the power rating of the device. Position the power cord so that people cannot step on it.

Page 7 If any of the following situations arises, please the contact our service personnel: Damaged power cord or plug Liquid intrusion to the device iii. Exposure to moisture Device is not working as expected or in a manner as described in this manual The device is dropped or damaged Any obvious signs of damage displayed on the device...

Page 8 FCC Statement This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Page 9 China RoHS Requirements (CN) 产品中有毒有害物质或元素名称及含量 AAEON Main Board/ Daughter Board/ Backplane 有毒有害物质或元素 部件名称 铅 汞 镉 六价铬 多溴联苯 多溴二苯醚 (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) 印刷电路板 ○ ○ ○ ○ 及其电子组件 外部信号 ○ ○ ○ ○ 连接器及线材 O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。 X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出...

Page 10 China RoHS Requirement (EN) Poisonous or Hazardous Substances or Elements in Products AAEON Main Board/ Daughter Board/ Backplane Poisonous or Hazardous Substances or Elements Hexavalent Polybrominated Polybrominated Component Lead Mercury Cadmium Chromium Biphenyls Diphenyl Ethers (Pb) (Hg) (Cd) (Cr(VI)) (PBB) (PBDE) PCB &...

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Page 15: Chapter 1 - Product Specifications

Chapter 1 Chapter 1 - Product Specifications...

Page 16: Specifications

Specifications System Form Factor PICO-ITX Intel Atom® x7000E Series, Intel® Processor N-series, and Intel® Core™ i3 Processor N-series Processors: Intel® Processor N50 (2C, 1.00 GHz, 6W) Intel® Processor N97 (4C, 2.00 GHz, 12W) Intel® Core™ i3-N305 (8C, 1.80 GHz, 15W) Intel Atom®...

Page 17 Power Power Consumption Intel® Core™ i3-N305, DDR5 32GB x 1, 2.97A @+12V (Typical) Intel® Core™ i3-N305, DDR5 32GB x 1, 4.46A @+12V (Max) Display Controller Intel® UHD Graphics for 12th Gen Intel® Processors LVDS x 1, Dual Channel 18/24-bit, 1920 x 1200 @60Hz LVDS/eDP eDP 1.4 x 1, 7680 x 4320 (Optional) Display Interface...

Page 18 Internal I/O Video LVDS/eDP x 1 (Default: LVDS) Inverter x 1 (12V/2A) SATA SATA 6Gb/s x 1 +5V SATA Power Connector x 1 Audio Line-out Header x 1 (Optional) DIO/GPIO GPIO 4-bit SMBus/I2C SMBus/I2C x 1 (Default: SMBus) Touch ━ 4-pin Smart Fan x 1 ━...

Page 19: Function Block Diagram

Function Block Diagram Chapter 1 – Product Specifications...

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Page 24: List Of Jumpers

List of Jumpers Jumpers allow users to manually customize system configurations to their suitable application needs. Please refer to the table below for all of the board’s jumpers that you can configure for your application Label Function Clear CMOS Jumper & Auto Power Button Enable/Disable 2.3.1 Clear CMOS Jumper &...

Page 25: List Of Connectors

List of Connectors Please refer to the table below for all of the board’s connectors that you can configure for your application Label Function RTC Battery Connector HDMI LVDS Back Light Inverter LVDS/eDP Dual RJ-45 LAN (Left I226-V/Right RTL8111H-CG) SATA Connector SATA Power Connector 4-bit GPIO Mini Card/mSATA...

Page 26: Rtc Battery Connector (Cn1)

2.4.1 RTC Battery Connector (CN1) Pin Name Signal Type Signal Level +3.3V +3.3V 2.4.2 HDMI (CN2) Pin Name Signal Type Signal Level HDMI_TX2+ DIFF HDMI_TX2- DIFF HDMI_TX1+ DIFF Chapter 2 – Hardware Information...

Page 27: Lvds Back Light Inverter (Cn3)

Pin Name Signal Type Signal Level HDMI_TX1- DIFF HDMI_TX0+ DIFF HDMI_TX0- DIFF HDMI_CLK+ DIFF HDMI_CLK- DIFF DDC_CLK Signal DDC_DATA Signal HDMI_HPD 2.4.3 LVDS Back Light Inverter (CN3) Pin Name Signal Type Signal Level BLK_PWR +12V (Default) / +5V BLK_PWR +12V (Default) / +5V BKL_CONTROL Signal Chapter 2 –...

Page 28: Lvds/Edp (Cn4)

Pin Name Signal Type Signal Level BKL_ENABLE Signal Note: Backlight power can be 12V or 5V by BOM. Stuff R307 for 12V and stuff R308 for 5V. [Default:12V]. Note: CN3 power current max: 2A. 2.4.4 LVDS/eDP (CN4) Pin Name Signal Type Signal Level LVD1_CB_3_DP DIFF...

Page 29 Pin Name Signal Type Signal Level +V3P3S +3.3V LVD1_DDC_CLK/ Signal DDI0_HPD LVD1_BKLTEN/ Signal DDI0_BKLTEN LVD1_DDC_DATA Signal LVD1_BKLCTL/ Signal

DDI0_BKLTCTL LVD1_CA_CLKP/ DIFF DDI0_AUX_DP LVD1_CA_CLKN/ DIFF DDI0_AUX_DN LVD1_CA_3_DP/ DIFF DDI0_LANE3_DP LVD1_CA_3_DN/ DIFF DDI0_LANE3_DN LVD1_CA_0_DP/ DIFF DDI0_LANE0_DP LVD1_CA_0_DN/ DIFF DDI0_LANE0_DN LVD1_CA_1_DP/ DIFF DDI0_LANE1_DP LVD1_CA_1_DN/ DIFF DDI0_LANE1_DN...

Page 30: Dual Rj-45 Lan (Cn5)

Pin Name Signal Type Signal Level +VDD +3.3V +VDD +3.3V Note: CN4: VDD power current max: 1.5A. 2.4.5 Dual RJ-45 LAN (CN5) Pin Name Pin Name LAN2_MDI0_P LAN1_MDI0_P LAN2_MDI0_N LAN1_MDI0_N LAN2_MDI1_P LAN1_MDI1_P LAN2_MDI1_N LAN1_MDI1_N 1CT5 2CT5 1CT6 2CT6 LAN2_MDI2_P LAN1_MDI2_P LAN2_MDI2_N LAN1_MDI2_N LAN2_MDI3_P...

Page 31: Sata Connector (Cn6)

2.4.6 SATA Connector (CN6) Pin Name Signal Type Signal Level SATA_1_TXP DIFF SATA_1_TXN DIFF SATA_1_RXN DIFF SATA_1_RXP DIFF 2.4.7 SATA Power Connector (CN7) Pin Name Signal Type Signal Level +V5S Note: CN7 SATA power current max: 1.5A. Chapter 2 – Hardware Information...

Page 32: 4-Bit Gpio Header (Cn8)

2.4.8 4-bit GPIO Header (CN8) Pin Name Signal Type Signal Level +V5S GPIO_0 Signal GPIO_1 Signal GPIO_2 Signal GPIO_3 Signal Note: CN8 GPIO power current max: 0.5A. Chapter 2 – Hardware Information...

Page 33: Mini Card/Msata (Cn9)

2.4.9 Mini Card/mSATA (CN9) Pin Name Signal Type Signal Level PCIE_WAKE# Signal +3.3V +3.3V +1.5V +1.5V PCIE_CLK_REQ# Signal PCIE_REF_CLK- DIFF PCIE_REF_CLK+ DIFF Chapter 2 – Hardware Information...

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Pin Name Signal Type Signal Level W_DISABLE# Signal +3.3V PCIE_RST# Signal +3.3V PCIE_RX-/SATA_RX+ DIFF +3.3V +3.3V PCIE_RX+/SATA_RX- DIFF +1.5V +1.5V SMB_CLK Signal +3.3V PCIE_TX-/SATA_TX- DIFF SMB_DATA Signal +3.3V PCIE_TX+/SATA_TX+ DIFF USB_D- DIFF USB_D+ DIFF +3.3V +3.3V +3.3V +3.3V Chapter 2 – Hardware Information...

Page 35: Dual Usb 3.2 Port (Cn11)

2.4.10 Dual USB 3.2 Port (CN11) Pin Name Signal Type Signal Level +V5A_USB12 +5V(0.9A) USB2_0_DN DIFF USB2_0_DP DIFF USB3_0_RXN DIFF USB3_0_RXP DIFF USB3_0_TXN DIFF USB3_0_TXP DIFF +V5A_USB12 +5V(0.9A) USB2_1_DN DIFF USB2_1_DP DIFF USB3_1_RXN DIFF USB3_1_RXP DIFF USB3_1_TXN DIFF USB3_1_TXP DIFF Note: USB 3.2 power current max: 0.9A.

Page 36: Dual Usb 2.0 Port (Cn12)

2.4.11 Dual USB 2.0 Port (CN12) Pin Name Signal Type Signal Level +5VSB(0.5A) +5VSB(0.5A) USB5_D- USB6_D- USB5_D+ USB6_D+ Note: USB 2.0 power current max: 0.5A. 2.4.12 SPI (For BIOS) (CN15) Pin Name Signal Type Signal Level SPI_SO Signal Chapter 2 – Hardware Information...

Page 37: 4-Pin Fan (Cn16)

Pin Name Signal Type Signal Level SPI_CLK Signal +V3P3A_SPI 3.3A SPI_SI Signal SPI_CS Signal 2.4.13 4-Pin Fan (CN16) Pin Name Signal Type Signal Level +V12S +12V FAN_TAC Signal FAN_CTL Signal Note: CN16 Smart fan power current max: 1.0A. Chapter 2 – Hardware Information...

Page 38: I2C/Smbus (Cn17)

2.4.14 I2C/SMBus (CN17) Pin Name Signal Type Signal Level +V3P3A/+V3P3S +3.3V SMB_CLK/I2C_CLK IN/OUT +3.3V SMB_DATA/I2C_DATA +3.3V SMBALERT#/INT +3.3V _SERIRQ +3.3V 2.4.15 eSPI Debug Connector (CN18) Pin Name Signal Type Signal Level ESPI_IO0 Signal +1.8V ESPI_IO1 Signal +1.8V ESPI_IO2 Signal +1.8V ESPI_IO3 Signal +1.8V...

Page 39: Bio (Cn20)

Pin Name Signal Type Signal Level +V3.3S +3.3V ESPI_CS Signal ESPI_RESET# Signal +1.8V ESPI_CLK Signal 1.8V +V3P3A Signal +3.3V 2.4.16 BIO (CN20) Pin Name Signal Type Signal Level +V12A +12V PCIE_0_TXN DIFF PCIE_0_RXN DIFF PCIE_0_TXP DIFF PCIE_0_RXP DIFF

PCIE_1_TXN DIFF PCIE_1_RXN DIFF PCIE_1_TXP...

Page 40 Pin Name Signal Type Signal Level +V5A +V5A +V5A +V5A PCIE_1_CLK_DP DIFF BUF_PLT_RST# Signal PCIE_1_CLK_DN DIFF DDI1_LANE1_DN DIFF DDI1_LANE0_DN DIFF DDI1_LANE1_DP DIFF DDI1_LANE0_DP DIFF DDI1_LANE3_DN DIFF DDI1_LANE2_DN DIFF DDI1_LANE3_DP DIFF DDI1_LANE2_DP DIFF DDI1_HPD_BIO Signal DDI1_AUXN DIFF DDI1_AUXP DIFF USB3_2_TXN DIFF USB3_2_TXP DIFF Chapter 2 –...

Page 41 Pin Name Signal Type Signal Level USB2_6_DN DIFF USB2_6_DP DIFF USB3_2_RXN DIFF USB3_2_RXP DIFF SMB_CLK SMB_DATA PCIE_WAKE# Signal USB2_OC2# Signal USB 2.0_OC# Signal LPC_AD0 Signal LPC_FRAME# Signal LPC_AD1 Signal SERIRQ# Signal LPC_AD2 Signal LPC_AD3 Signal GPIO Signal Audio_GND Chapter 2 – Hardware Information...

Page 42: Front Panel (Cn22)

Pin Name Signal Type Signal Level LPC_CLK Signal Audio_OUT_L Signal PME# Signal Audio_OUT_R Signal 2.4.17 Front Panel (CN22) Pin Name Signal Type Signal Level EXT_PWRBTN# Signal FP_IDELED# Signal +V3P3S +3.3V FP_BUZZER Signal +V5S +V3P3S +3.3V HWRST# Signal Chapter 2 – Hardware Information...

Page 43: Power Input +12V (Cn23)

2.4.18 Power Input +12V (CN23) Pin Name Signal Type Signal Level +V_IN +12V 2.4.19 DC Jack Power Input [Reserved] (CN24) Pin Name Signal Type Signal Level +V_IN +12V Chapter 2 – Hardware Information...

Page 44: Com Port (Cn26)

2.4.20 COM Port (CN26) Pin Name Signal Type Signal Level DCD_1 TX_1- DATA_1- DCD_2 TX_2- DATA_2- RX_1 TX_1+ DATA_1+ RX_2 TX_2+ DATA_2+ TX_1 RX_1+ TX_2 RX_2+ DTR_1 RX_1- DTR_2 RX_2- DSR_1 DSR_2 RTS_1 RTS_2 CTS_1 CTS_2 RI_1/12V/5V RI_2/12V/5V Chapter 2 – Hardware Information...

Page 45: Audio Connector (Cn28)

Pin Name Signal Type Signal Level UART_TX UART_RX Note: COM RS-232/422/485 can be set by BIOS setting. Default is RS-232. Note: RI1/+5V/+12V function can be set by BOM(R556-RI/R554-+12V/R555-+5V). Default is RING. Note: RI2/+5V/+12V function can be set by BOM(R562-RI/R560-+12V/R561-+5V). Default is RING. Note: CN26 COM power current max: 0.5A for each port.

Page 46: Thermal Assembly Options

Thermal Assembly Options 2.5.1 Fanless Heatspreader/Heatsink Heatspreader, Part Number: PICO-ADN4-HSP01. Heatsink, Part Number: PICO-ADN4-HSK01. SCREW :M 3x6mmL (PICO-ADN4-HSK01 ACCESSORIES) PICO-ADN4-HSK01 PICO-ADN4-HSP01 Before installing heat sink, please apply thermal grease COPPER STUD,M 3x6.5+5mm at this area. (PICO-ADN4-HSP01 ACCESSORIES) PICO-ADN4 M 3.0 Internal Thread CHASSIS (Parts are subject to customer's assembly method)

Page 47: Chapter 3 - Ami Bios Setup

Chapter 3 Chapter 3 - AMI BIOS Setup...

Page 48: System Test And Initialization

System Test and Initialization These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

Page 49: Ami Bios Setup

AMI BIOS Setup AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off. Entering Setup Power on the computer and press <Del>or <ESC>...

Page 50: Setup Submenu: Main

Setup Submenu: Main Chapter 3 – AMI BIOS Setup...

Page 51: Setup Submenu: Advanced

Setup Submenu: Advanced Chapter 3 – AMI BIOS Setup...

Page 52: Cpu Configuration

3.4.1 CPU Configuration Options Summary Intel (VMX) Virtualization Disabled Technology Enabled Optimal Default, Failsafe Default When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. Intel® SpeedStep™ Disabled Enabled Optimal Default, Failsafe Default Allows more than two frequency ranges to be supported. Turbo Mode Disabled Enabled...

Page 53: Pch-Fw Configuration

3.4.2 PCH-FW Configuration Chapter 3 – AMI BIOS Setup...

Page 54: Firmware Update Configuration

3.4.2.1 Firmware Update Configuration Options Summary Me FW Image Re-Flash Enabled Disabled Optimal Default, Failsafe Default Enable/Disable Me FW Image Re-Flash function. FW Update Disabled Enabled Optimal Default, Failsafe Default Enable/Disable ME FW Update function. Chapter 3 – AMI BIOS Setup...

Page 55: Ptt Configuration

3.4.3 PTT Configuration Options Summary TPM Device Selection dTPM Optimal Default, Failsafe Default Selects TPM device: PTT or discrete TPM. PTT - enables PTT in SkuMgr. dTPM - disables PTT in SkuMgr. Warning! PTT/dTPM will be disabled and all data saved on it will be lost. Chapter 3 –...

Page 56: Trusted Computing

3.4.4 Trusted Computing Options Summary Security Device Support Enable Optimal Default, Failsafe Default Disable Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. SHA256 PCR Bank Enabled Optimal Default, Failsafe Default Disabled...

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Options Summary Storage Hierarchy Enabled Optimal Default, Failsafe Default Disabled Enable or Disable Storage Hierarchy. Endorsement Hierarchy Enabled Optimal Default, Failsafe Default Disabled Enable or Disable Endorsement Hierarchy. Physical Presence Spec Optimal Default, Failsafe Default Version Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.

Page 58: Sata Configuration

3.4.5 SATA Configuration Options Summary SATA Controller(s) Enabled Optimal Default, Failsafe Default Disabled Enable/Disable SATA Device. Port 0 (CN10) Enabled Optimal Default, Failsafe Default Disabled Enable or Disable SATA Port. Port1(CN11)/mSATA (CN8) Enabled Optimal Default, Failsafe Default Disabled Enable or Disable SATA Port. Chapter 3 –...

Page 59: Hardware Monitor

3.4.6 Hardware Monitor Options Summary Smart Fan Disabled Enabled Optimal Default, Failsafe Default Enables or Disables Smart Fan. Chapter 3 – AMI BIOS Setup...

Page 60: Smart Fan Mode Configuration

3.4.6.1 Smart Fan Mode Configuration Options Summary Fan 1 Smart Fan Control Manual Duty Mode Auto Duty-Cycle Mode Optimal Default, Failsafe Default Smart Fan Mode Select Temperature Source CPU Temperature System Temperature Optimal Default, Failsafe Default System Temperature 2 Select the monitored temperature source for this fan. Temperature 1 Temperature 2 Temperature 3...

Page 61: Sio Configuration

3.4.7 SIO Configuration Chapter 3 – AMI BIOS Setup...

Page 62: Serial Port 1 Configuration

3.4.7.1 Serial Port 1 Configuration Options Summary Use This Device Disable Enable Optimal Default, Failsafe Default Enable or Disable this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=3F8h; IRQ=4 IO=2F8h; IRQ=3 Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.

Page 63: Serial Port 2 Configuration

3.4.7.2 Serial Port 2 Configuration Options Summary Use This Device Disable Enable Optimal Default, Failsafe Default Enable or Disable this Logical Device. Possible: Use Automatic Settings Optimal Default, Failsafe Default IO=2F8h; IRQ=3 IO=3F8h; IRQ=4 Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.

Page 64: Serial Port Console Redirection

3.4.7.3 Serial Port Console Redirection Options Summary Console Redirection Disabled Enabled Optimal Default, Failsafe Default Console Redirection Enable or Disable. Console Redirection EMS Disabled Optimal Default, Failsafe Default Enabled Console Redirection Enable or Disable. Chapter 3 – AMI BIOS Setup...

Page 65: Legacy Console Redirection Settings

3.4.7.4 Legacy Console Redirection Settings Options Summary Redirection COM port COM0 Optimal Default, Failsafe Default COM1(Pci Bus0, Dev0, Func0) (Disabled) Select a COM Port to display redirection of Legacy OS and Legacy OPROM message. Resolution 80x24 Optimal Default, Failsafe Default 80x25 On Legacy OS, the number of Rows and Columns supported redirection.

Page 66: Aaeon Bios Robot

3.4.8 AAEON BIOS Robot Options Summary Sends watch dog before Disabled Optimal Default, Failsafe Default BIOS POST Enabled Enabled - Robot set Watch Dog Timer (WDT) right after power on, before BIOS start POST process. And then Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to zero.

Page 67 Options Summary Delayed POST (PEI phase) Disabled Optimal Default, Failsafe Default Enabled Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this before 'Sends watch dog'.

Page 68: Device Detecting Configuration

3.4.8.1 Device Detecting Configuration Options Summary Action Reset System Optimal Default, Failsafe Default Hold System Select action that robot should do. Soft or hard reset Soft Optimal Default, Failsafe Default Hard Select reset type robot should send on each boot. Retry-Count Optimal Default, Failsafe Default Fill retry counter here.

Page 69 3.4.8.1.1 Device #1 Detecting Configuration Options Summary Interface Disable Optimal Default, Failsafe Default SMBUS Legacy I/O Super I/O MMIO Select interface robot should use to communicate with device. Chapter 3 – AMI BIOS Setup...

Page 70 3.4.8.1.2 Device #2 Detecting Configuration Options Summary Interface Disable Optimal Default, Failsafe Default SMBUS Legacy I/O Super I/O MMIO Select interface robot should use to communicate with device. Chapter 3 – AMI BIOS Setup...

Page 71 3.4.8.1.3 Device #3 Detecting Configuration Options Summary Interface Disable Optimal Default, Failsafe Default SMBUS Legacy I/O Super I/O MMIO Select interface robot should use to communicate with device. Chapter 3 – AMI BIOS Setup...

Page 72 3.4.8.1.4 Device #4 Detecting Configuration Options Summary Interface Disable Optimal Default, Failsafe Default SMBUS Legacy I/O Super I/O MMIO Select interface robot

should use to communicate with device. Chapter 3 – AMI BIOS Setup...

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3.4.8.1.5 Device #5 Detecting Configuration Options Summary Interface Disable Optimal Default, Failsafe Default SMBUS Legacy I/O Super I/O MMIO Select interface robot should use to communicate with device. Chapter 3 – AMI BIOS Setup...

Page 74: Power Management

3.4.9 Power Management Options Summary Power Mode ATX Type Optimal Default, Failsafe Default AT Type Select power supply mode. Restore AC Power Loss Last State Optimal Default, Failsafe Default Always On Always Off Select power state when power is re-applied after a power failure. Soft-Off (S5) Wake On RTC Disable Optimal Default, Failsafe Default By Date...

Page 75: Gpio Port Configuration

3.4.10 GPIO Port Configuration Options Summary GPIO Port* Output Input Set GPIO as Input or Output. Output Level High Set output level when GPIO pin is output. Chapter 3 – AMI BIOS Setup...

Page 76: Aaeon Smart Boost

3.4.11 AAEON Smart Boost Options Summary AAEON Smart Boost Smart Boost Maximum Performance Good Stability Disabled Optimal Default, Failsafe Default Chapter 3 – AMI BIOS Setup...

Page 77: Setup Submenu: Chipset

Setup Submenu: Chipset Chapter 3 – AMI BIOS Setup...

Page 78: System Agent (Sa) Configuration

3.5.1 System Agent (SA) Configuration Options Summary VT-d Disabled Optimal Default, Failsafe Default Enabled VT-d capability. Chapter 3 – AMI BIOS Setup...

Page 79: Memory Configuration

3.5.1.1 Memory Configuration Chapter 3 – AMI BIOS Setup...

Page 80: Lvds Panel Configuration

3.5.1.2 LVDS Panel Configuration Options Summary LVDS Disabled Enabled Optimal Default, Failsafe Default Enable/Disable this panel. LVDS Panel Type 640x480,18bit,60Hz 800x480,18bit,60Hz 800x600,18bit,60Hz 1024x600,18bit,60Hz 1024x768,18bit,60Hz 1024x768,24bit,60Hz Optimal Default, Failsafe Default 1280x768,24bit,60Hz 1280x1024,48bit,60Hz 1366x768,24bit,60Hz 1440x900,48bit,60Hz 1600x1200,48bit,60Hz 1920x1080,48bit,60Hz 1920x1200,48bit,60Hz Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.

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Options Summary Color Depth 18-bit Optimal Default, Failsafe Default 24-bit 36-bit 48-bit Select panel type. Backlight Mode BIOS & Application Windows Slider Optimal Default, Failsafe Default Select backlight control signal type. Chapter 3 – AMI BIOS Setup...

Page 82: Pch-Io Configuration

3.5.2 PCH-IO Configuration Options Summary HD Audio Disabled Enabled Optimal Default, Failsafe Default Control Detection of the HD-Audio device. Disable = HAD will be unconditionally disabled. Enable = HAD will be unconditionally enabled. Full-MiniCard Slot Function SATA Optimal Default, Failsafe Default (CN9) PCIe Select function enabled for Full-MiniCard (CN9) slot.

Page 83: Setup Submenu: Security

Setup Submenu: Security Change User/Supervisor Password You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility. If you highlight these items and press Enter, a dialog box appears which lets you enter a password.

Page 84: Secure Boot

3.6.1 Secure Boot Options Summary Secure Boot Disabled Optimal Default, Failsafe Default Enabled Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled

and the System is in User mode. The mode change requires platform reset. Secure Boot Mode Custom Optimal Default, Failsafe Default...

Page 85: Key Management

3.6.1.1 Key Management Options Summary Factory Key Provision Disabled Optimal Default, Failsafe Default Enabled Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset. Restore Factory Keys Force System to User Mode.

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Options Summary Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db). Restore DB defaults Restore DB variable to factory defaults. Platform Key (PK) Update Key Exchange Keys Update Append Authorized Signatures Update Append Forbidden Signatures Update Append...

Page 87: Setup Submenu: Boot

Setup Submenu: Boot Options Summary Quiet Boot Disabled Enabled Optimal Default, Failsafe Default Enable or Disable Quiet Boot option. UEFI PXE Support Disabled Optimal Default, Failsafe Default Enabled Enable/Disable UEFI Network Stack. FIXED BOOT ORDER Priorities Sets the system boot order. Chapter 3 –...

Page 88: Bbs Priorities

3.7.1 BBS Priorities Chapter 3 – AMI BIOS Setup...

Page 89: Setup Submenu: Save & Exit

Setup Submenu: Save & Exit Options Summary Save Changes and Reset Reset the system after saving the changes. Discard Changes and Exit Exit system setup without saving any changes. Restore Defaults Restore/Load Default values for all the setup options. Chapter 3 – AMI BIOS Setup...

Page 90: Chapter 4 - Drivers Installation

Chapter 4 Chapter 4 – Drivers Installation...

Page 91: Drivers Download And Installation

Drivers Download and Installation Drivers for the PICO-ADN4 can be downloaded from the product page on the AAEON website by following this link: https://www.aaeon.com/ Download the driver(s) you need and follow the steps below to install them. Install Chipset Driver Open the Intel Chipset folder.

Page 92

Run the Setup.exe file Follow the instructions Driver will be installed automatically Install ME Driver Open the ME folder. Run the SetupME.exe file Follow the instructions Driver will be installed automatically Install Serial IO Driver Open the Serial IO folder. Follow the instructions in the .inf files to manually install drivers.

Page 93: Appendix A - Mating Connectors

Appendix A Appendix A – Mating Connectors...

Page 94: List Of Mating Connectors And Cables

List of Mating Connectors and Cables The following table lists mating connectors and available cables. Mating Connector AAEON Label Function Available Cable Cable P/N Vendor Model No. RTC Battery Molex 51021-0200 Battery Cable 175011301K LVDS Back Light SHR-06V-S-B LVDS Inverter Inverter Cable LVDS...

Page 95: Appendix B - I/O Information

Appendix B Appendix B - I/O Information...

Page 96: I/O Address Map

I/O Address Map Appendix B – I/O Information...

Page 97: Irq Mapping Chart

IRQ Mapping Chart Appendix B – I/O Information...

Page 98 Appendix B – I/O Information...

Page 99 Appendix B – I/O Information...

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Page 106 Appendix B – I/O Information...

Page 107 Appendix B – I/O Information...

Page 108: Large Memory Map

Large Memory Map Memory Address Map Appendix B – I/O Information...

Page 109: Appendix C - Watchdog Timer Programming

Appendix C Appendix C - Watchdog Timer Programming...

Page 110: Introduction To Watchdog Timer

Introduction to Watchdog Timer This section details how to set up and program the Watchdog Timer for your AAEON system or board. The watchdog timer is used to automatically detect malfunctions and recover the system. During normal operation, the system will regularly send a signal to reset the watchdog timer.

Page 111: C.2 Programing The Watchdog Timer With Aaeon Sdk

C.2 Programing the Watchdog Timer with AAEON SDK If you have installed the AAEON Framework, you can program the Watchdog Timer using the AAEON SDK. Simply locate where the SDK is installed, and double click the icon. The following dialog box will appear: Count Mode: Set Watchdog Timer to count in minutes or seconds.

Page 112: C.3 Programing Watchdog Timer With Aaeon Windows Eapi

C.3 Programing Watchdog Timer with AAEON Windows EAPI AAEON Framework (KMDF Driver) must be installed before calling these functions. EapiLibInitialize() should be the first to call before calling other EAPI functions. EApiLibUnInitialize() should be called to release resources before program exit.

Page 113: Watchdog Timer Functions

EApiWDogStop must be called before Stage C/F to prevent event from being generated. EApiWDogStop must be called before Stage D/G to prevent system from being reset. C.3.1 Watchdog Timer Functions C.3.1.1 EapiWDogGetCap() Command Line: EApiWDogGetCap(...) __OUTOPT uint32_t *pMaxDelay, __OUTOPT uint32_t *pMaxEventTimeout, __OUTOPT uint32_t *pMaxResetTimeout Use this command to get maximum Supported Delay / Supported Event Timeout / Supported Reset Timeout of the watchdog timer.

Page 114: Eapiwdogstart()

C.3.1.2 EapiWDogStart() Command Line: EApiWDogStart(__IN uint32_t Delay, __IN uint32_t Minute, __IN uint32_t EventTimeout, __IN uint32_t ResetTimeout Use this command to start the

Watchdog Timer and set the timeout values. To stop the Watchdog Timer, issue the command EApiWDogStop. After issuing EAPiWDogStop, the command EApiWDogStart must be called again with new values to restart.

Page 115: Eapiwdogtrigger()

C.3.1.3 EapiWDogTrigger() Command Line: EapiWDogTrigger() Use this command to trigger the Watchdog Timer. Parameters Function Parameters None Condition Return Values Library Uninitialized EAPI_STATUS_NOT_INITIALIZED Watchdog Not Started EAPI_STATUS_ERROR Common Error Common Error Code Others EAPI_STATUS_SUCCESS C.3.1.4 EapiWDogStop() Command Line: EapiWDogStop() Use this command to close the Watchdog Instance. This will disable the Watchdog Timer and clear previous settings.

Page 116: Eapiwdogreloadtimer()

C.3.1.5 EapiWDogReloadTimer() Command Line: EapiWDogReloadTimer() Use this command to reload the Timeout count Parameters Function Parameters None Condition Return Values Library Uninitialized EAPI_STATUS_NOT_INITIALIZED Common Error Common Error Code Others EAPI_STATUS_SUCCESS C.3.1.6 EapiWDogGetStatus() Command Line: EapiWDogGetStatus(__OUTOPT uint32_t *pwdtMinute, __OUTOPT uint32_t *pwdtCountTime, __OUTOPT uint32_t *pwdtReloadTime Use this command to get the Watchdog Timer mode, time count value and reload timer.

Page 117: Eapiwdogsetstatus

C.3.1.7 EapiWDogSetStatus() Command Line: EApiWDogSetStatus(__IN uint32_t wdtMinute, __IN uint32_t wdtCountTime, __IN uint32_t wdtReloadTime Use this command to set Watchdog Timer mode, time count value and reload timer. Parameters Function Parameters wdtMinute Set the mode of minute or second wdtCountTime Set WDT time count wdtReloadTime Set WDT ReloadTime...